Final Report

for

Conversion - Regulation from Unconventional Primary and Secondary Sources

(23 June 1967 - 23 June 1969)

Contract No.: NAS-5-10440

Prepared by

Honeywell Inc.
Ordnance Division
Hopkins, Minnesota 55343

for

Goddard Space Flight Center

Greenbelt, Maryland

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SUMMARY

This report describes technical details of work completed during the contract period of contract NAS-5-10440. The object of this program is to develop a power conditioner of minimum size and weight which will derive power from a radioisotope thermoelectric generator and maintain high performance over a variable load profile, while efficiently converting the low RTG voltage to a higher level. This power conditioner includes a secondary source (silver-zinc battery) to supply peak load requirements in excess of the RTG's capabilities. It also includes two low-voltage converters, a battery charging circuit, a battery sequencing circuit, and associated circuitry to provide the proper logic functions, voltage and current regulation, and high performance over the wide operating ranges for a three-year space mission.

During the contract period, several system approaches were considered. The system selected consists of two separately powered inverters, the outputs of which are connected in parallel, which in turn are connected to a single output voltage regulator. This system was selected on the basis of being the least complex and most reliable of the systems considered. A block diagram for this system is shown in Figure 1. Block diagrams for the other systems considered are shown in Figures 2 through 5.

The two LIVC's, the output regulator, and the battery charging and sequencing circuits were designed separately and then connected to determine and correct interface problems. When the two LIVC's and output regulator were connected and operated, the biggest problem encountered was unstable operation due to system transients created by operation of the RTG overvoltage protection circuit. These transients were also the main source of problems when the battery charging and sequencing circuits were connected to the system. It should be noted that although the transients are created by operation of the RTG overvoltage protection circuit, there is no intention to infer poor design of this circuit. This circuit was retained in the system

design because it appears to be the least complex, low-loss approach that adequately limits the RTG voltage. Problems created by these transients have been overcome.

The battery charging and sequencing circuits were originally designed with discrete components. Much of the sequencing logic was later converted to integrated circuits. This resulted in significant reduction in size and complexity and a probable increase in system reliability. A computer program was written to determine optimum LIVC power transformer turns ratios for proper balance and load sharing of the two LIVC's. This program was used to verify original calculations and to facilitate study of use of another type RTG. The program is written so that the input voltages and impedances of both LIVC's can be varied and input currents and output voltages compared for different LIVC output transformer turns ratios.

Several new, possible significant developments were made during the contract period. The most significant of these includes a very stable voltage regulator; two unique, low-loss methods for sensing current in a pulse width-modulated system; and a simple system for using secondary current feedback for transistor drive in an inverter.

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I. TECHNICAL DISCUSSION

A. INTRODUCTION

The purpose of this program is to develop a power conditioning unit capable of operating from a radioisotope thermoelectric generator (RTG), and provide a variable load power output suitable for extending three-year space missions with high confidence and reliability levels. The scope of work includes the system analysis, load and interface investigations, and design and fabrication of a breadboard power conditioning unit to verify the feasibility and performance of this method of conditioning power.

Some unique properties of this system are that it consists of a RTG source and a silver-zinc battery cell source charged from the RTG, and serves as an auxiliary power source during peak load conditions. The battery source actually consists of four reserve-type silver-zinc cells selected and used, one at a time, in sequence. Each time the cell is degraded, another cell is activated and charged, and the degraded cell is switched out of the circuit. Of particular interest is the problem of paralleling the RTG, which has a relatively high source impedance. Two separate inverters, which feed into a common regulator, are being used.

The following discussions deal with work accomplished in the past two years, including recommendations and conclusions.

B. WORK ACCOMPLISHED

1. Circuit Design and Breadboard

a. Battery 90-Watt LIVC - When operating from a low-impedance battery it is of paramount importance that the LIVC does not draw current spikes when switching occurs or due to any unbalance in the LIVC operation. A circuit approach which tends to force a "double off" transistor switching condition in the LIVC is shown in Figure 6. The switching operation affected is very similar to that which would be characteristic if transformer T1

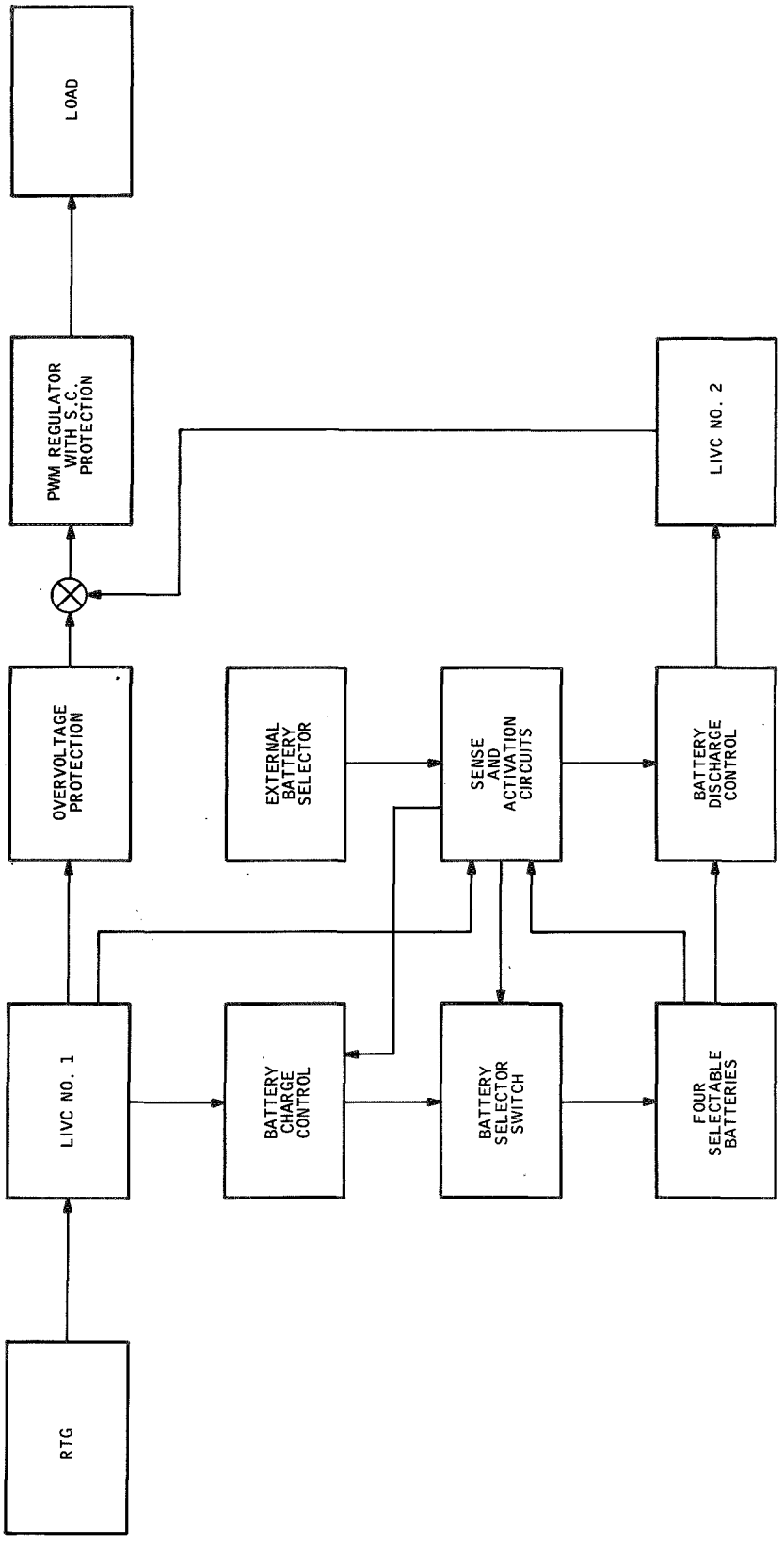


Figure 1. Configuration No. 1 Block Diagram

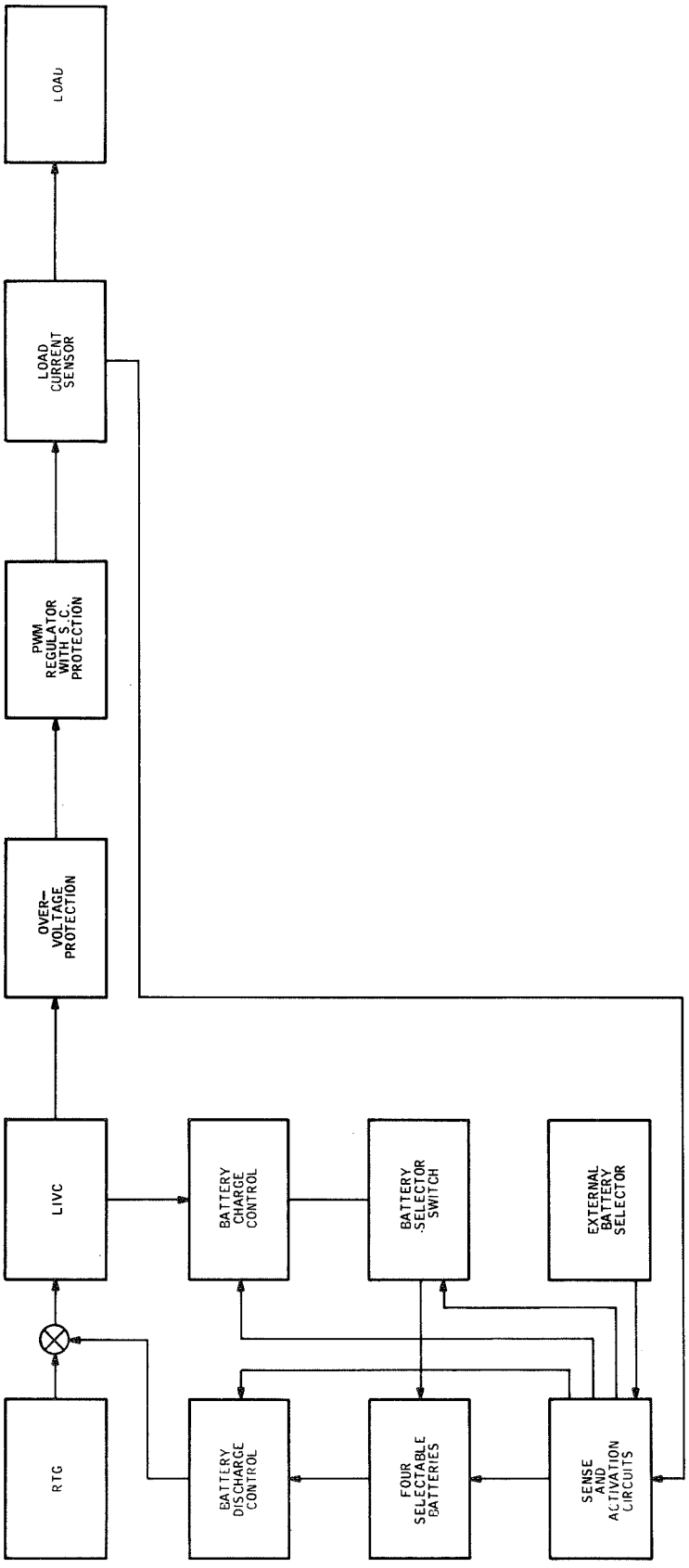


Figure 2. Configuration No. 2 Block Diagram

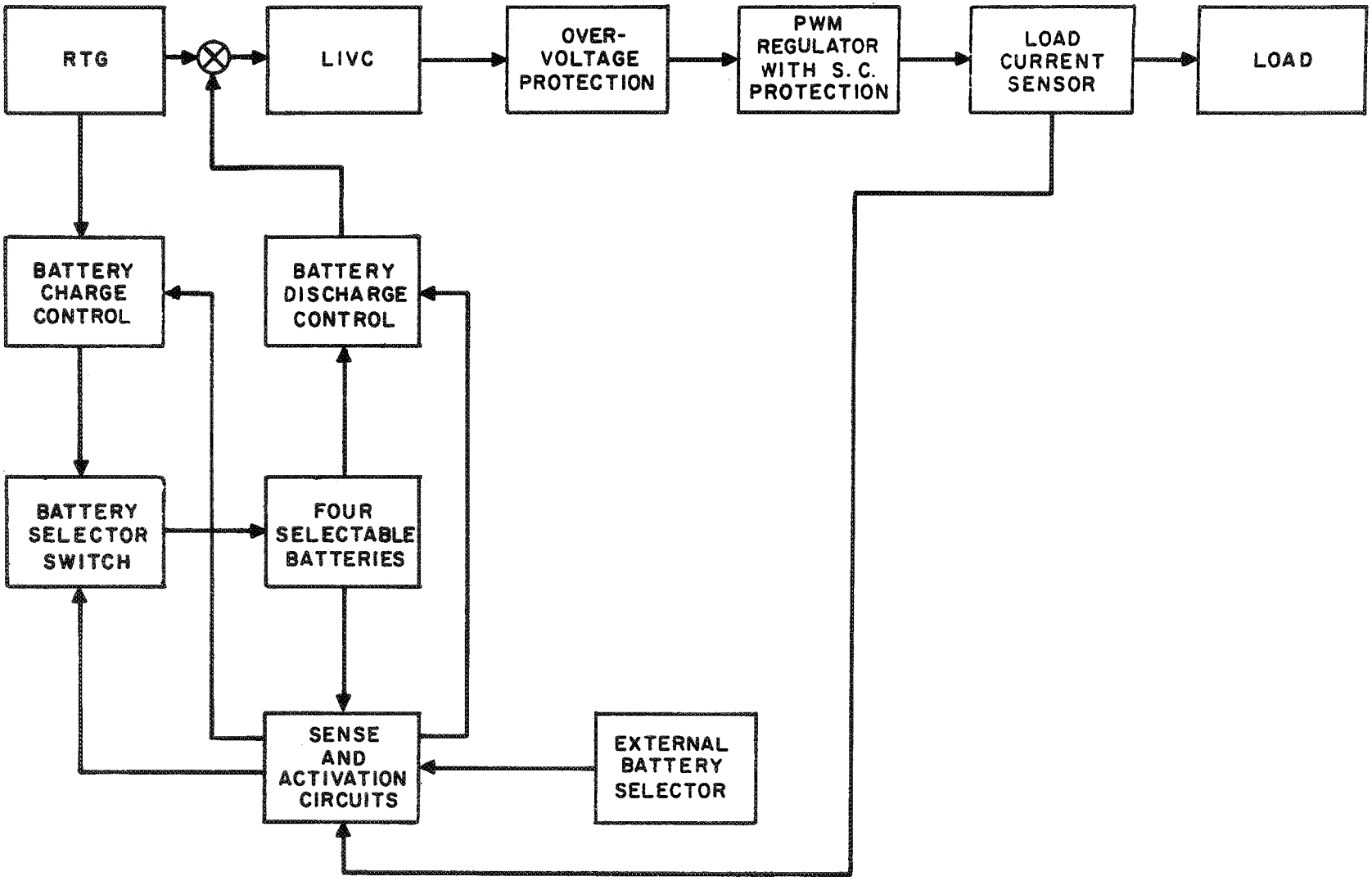


Figure 3. Configuration No. 3 Block Diagram

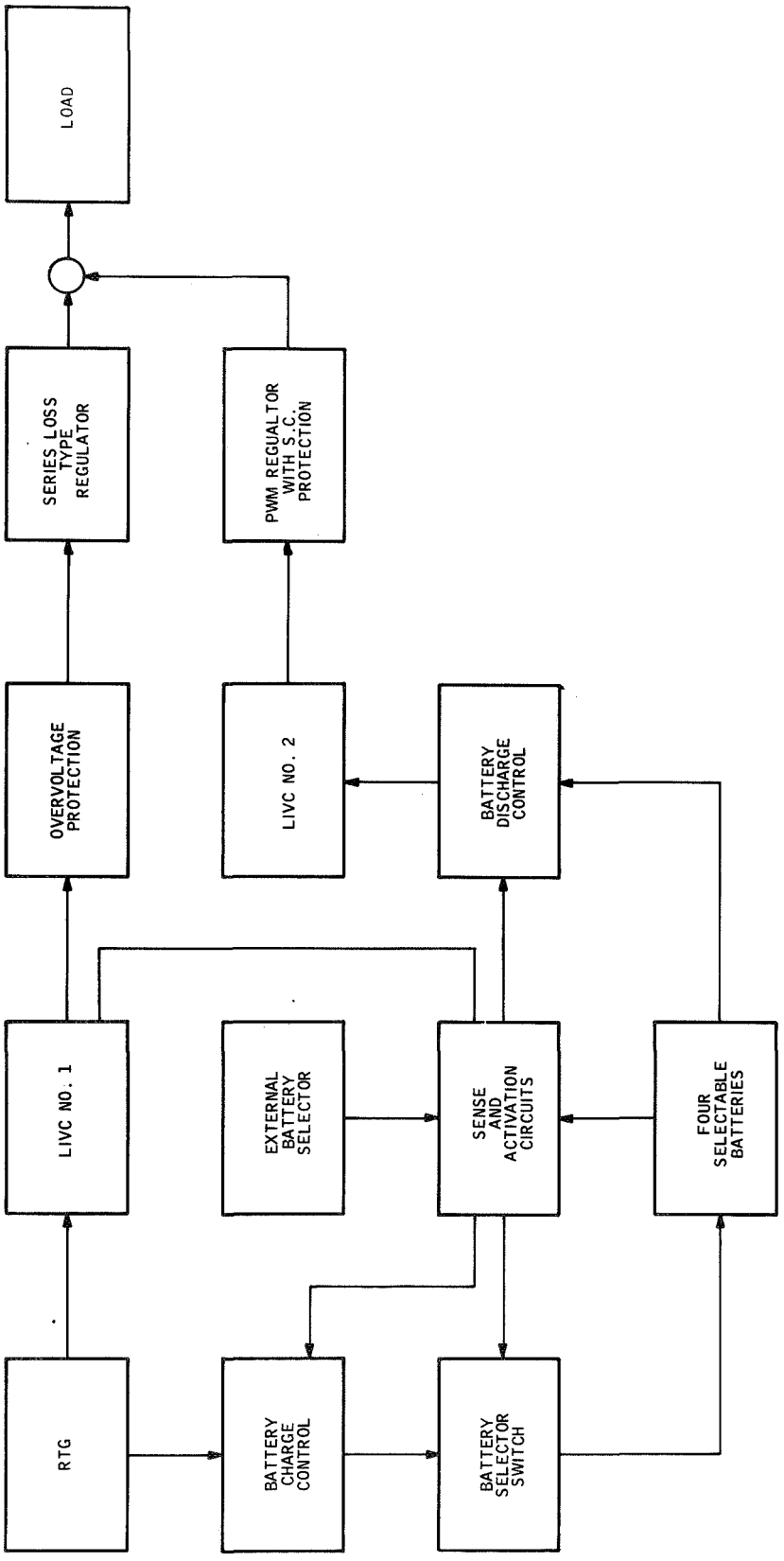


Figure 4. Configuration No. 4 Block Diagram

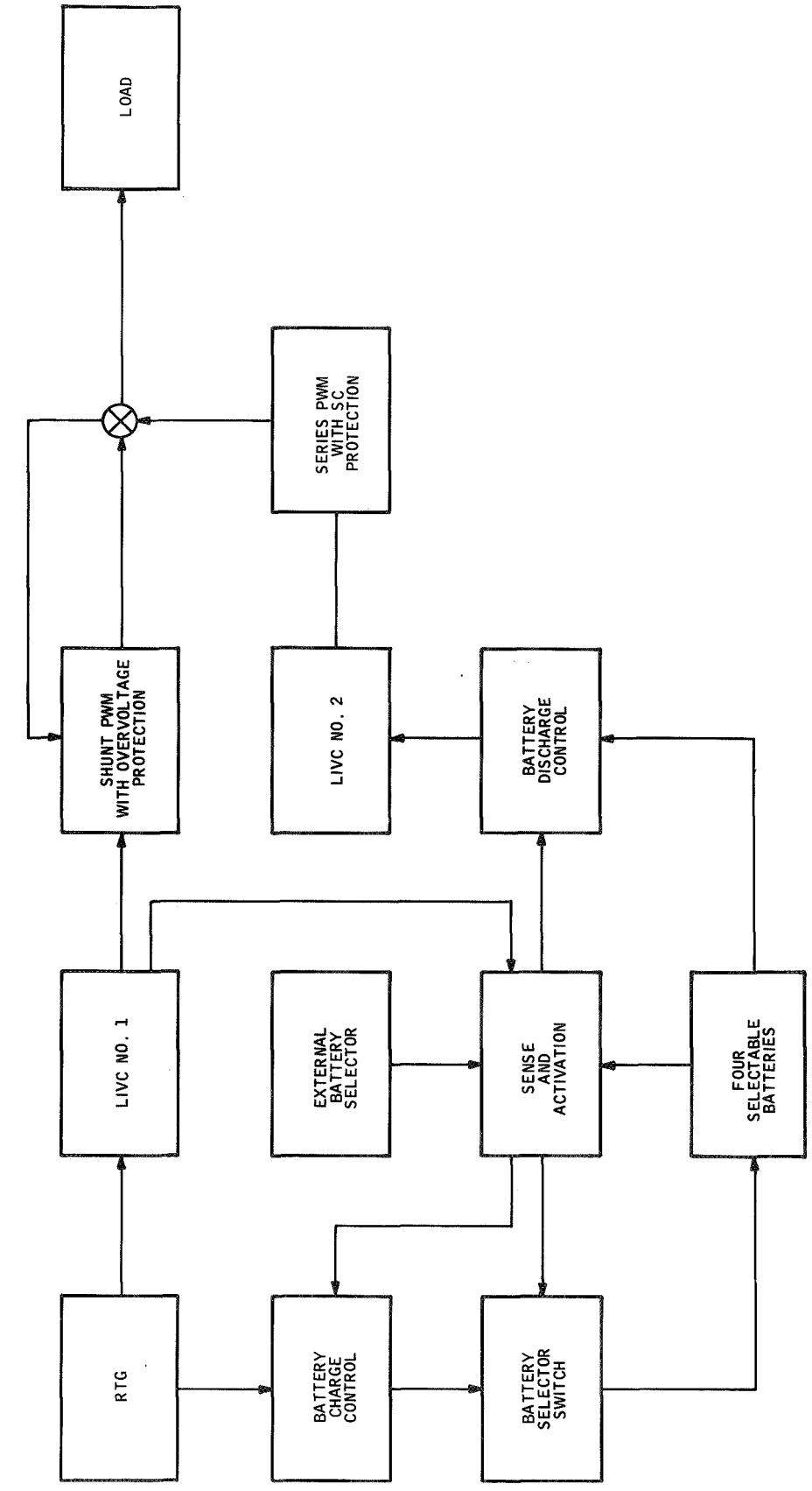


Figure 5. Configuration No. 5 Block Diagram

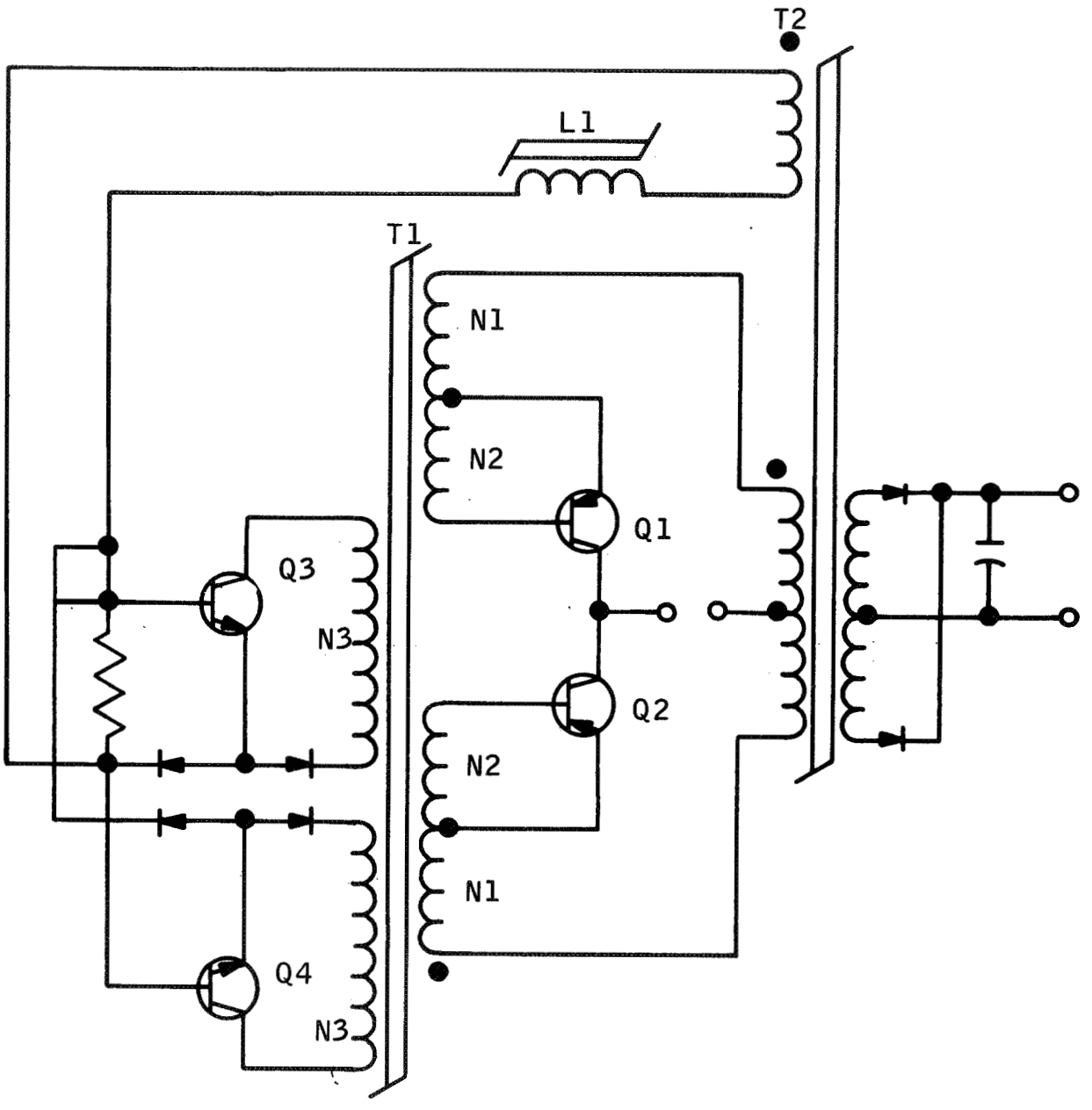


Figure 6. Experimental Drive Circuit for the 90-watt LIVC

were allowed to saturate and cause switching. In this condition, the transistor which was conducting is turned off when T1 saturates. The next transistor does not turn on until the previous transistor is completely off and the T1 core resets.

The intent of the indicated circuit is to effect that same basic operation by simulating core saturation with a turnon of transistors Q3 and Q4. The advantage of this circuit is that it enables the designer to control the frequency of the converter proportional with the input voltage to the LIVC. While this may not be a prime requirement, in situations when operating from the battery and the battery voltage is relatively constant, it does enable the designer to easily synchronize two converters which may possibly be connected redundantly.

Initial circuit investigations on this approach indicate it has some limitations. The major problem encountered was that complete switching was not realized before the transistors Q3 and Q4 would turn off. Therefore, while switching was initiated it was not completed, and a high frequency-type operation was encountered, or there would be only a momentary interruption in conduction and the final switching would not be effected until T1 actually saturated. In an attempt to realize more positive switching action, the transistors Q3 and Q4 were replaced with SCR's. However, this proved inadequate and additional work in the general area indicated this circuit approach is not feasible.

The circuit in Figure 7 shows another approach for minimizing or eliminating the "double on" problem. The switching frequency is controlled by L1, and the oscillator transistors Q3 and Q4 drive currents are supplied by current transformer T1. An additional current transformer, T2, is used to supply turnon and turnoff signals to transistors Q1 and Q2. Operation of this circuit is as follows: Assume transistor Q3 is on. Current flow through transformer T2 is in such a direction that it applies (through transformer action) drive current to transistor Q1 and reverse bias to the base to emitter junction of transistor Q2.

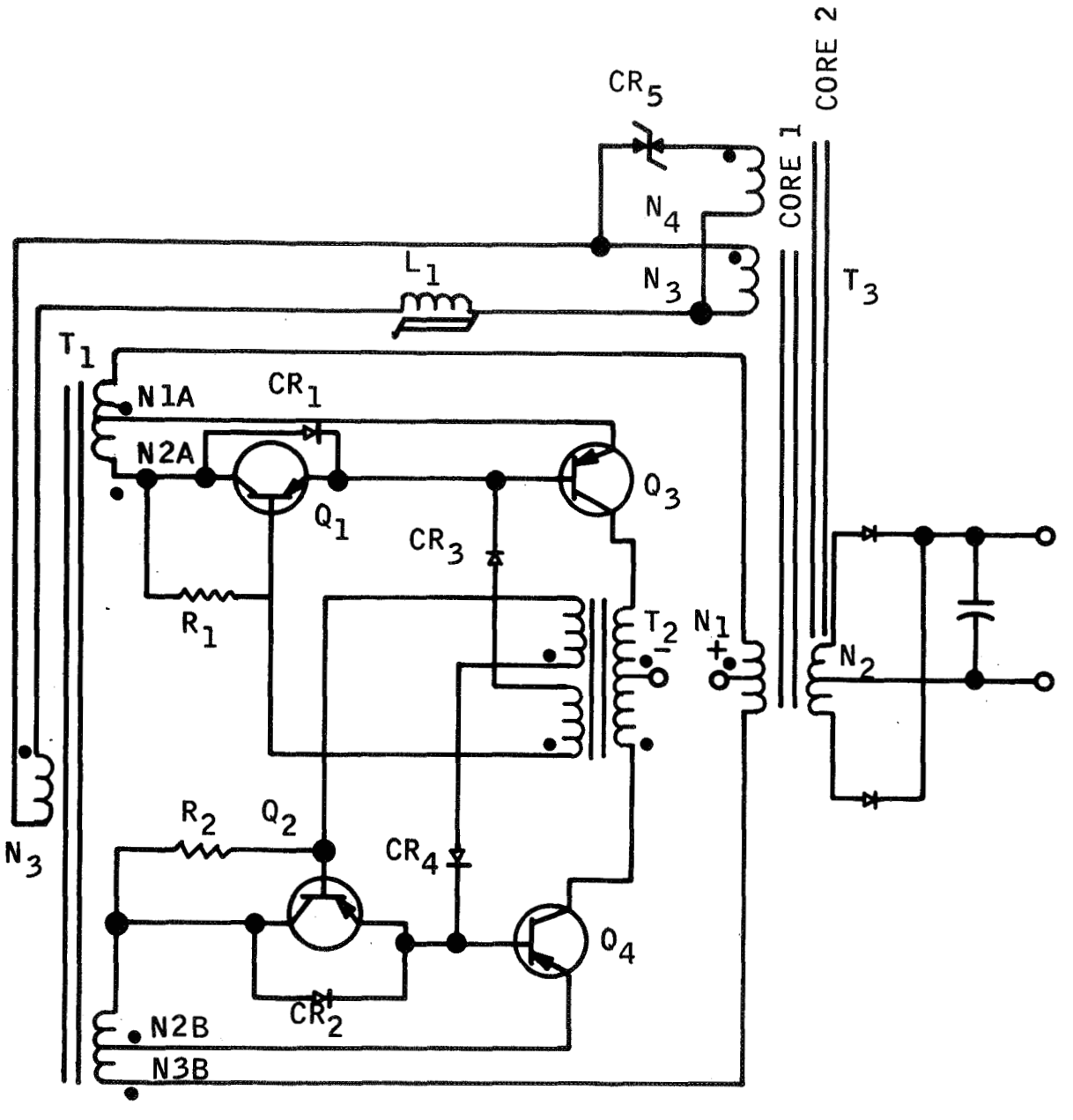


Figure 7. Possible Circuit for 90-watt LIVC

Inductor L1 saturates and applies a voltage to winding N3 of transformer T1. Phasing of this voltage is such that it applies a reverse bias on the base junction of Q3 from winding N2A through diode CR1. The base drive for transistor Q4 from winding N2B is blocked by transistor Q2 until the current through Q3 drops to a small value. Transistor Q2 will start turning on by base current through R2. Transistors Q2 and Q4 will then turn on fully from regenerative action through transformer T2. As soon as the L1 saturation occurs, a small drive current is applied to transistor Q4 through the transformer T2 secondary winding and R2. Current through R2 need only be large enough to turn on Q2 slightly so that regenerative action can take place. The same action occurs at the end of the next half cycle except that Q4 turns off and Q3 turns on. Diodes CR3 and CR4 prevent the secondary of transformer T2 from providing drive current to the off transistor through R1 or R2. This circuit is quite effective in eliminating "double on" time; however, the efficiency of the system is reduced by the extra losses in transistors Q1 and Q2 and transformer T2.

A method for minimizing "half cycle unbalance," described on page 42 of the proposal for this contract, used two high permeability cores having different coercive amp-turn requirements. The primary and secondary of the LIVC output transformer were wound around both cores. An additional series secondary was wound around the core with the highest coercivity requirement. Basically, the theory of operation of this system was that if the main core saturated, flux would flow in the second core. The second core would be reset on each half cycle by load current through the series winding. This system was tested and worked quite well. There was a slight increase in current when the first core saturated because of the higher magnetizing current of the second core; however, the increase in current was not great enough to cause damage. It was decided that a modification of this approach would be tried. The higher coercivity core with the series secondary will be replaced with a core that has an air gap and no extra winding. The air gap will reset the core on each half cycle. The

length of the air gap can be controlled by cutting a nominal length gap in the core, using a spacer of the proper width, and clamping the air gap to the spacer.

In Figure 7, core number 1 is a conventional core that would be used in a standard transformer design (in this case it is a 164E8602). Core number 2 is a high reluctance, self-resetting core (in this case it is a 5772L4 with an 0.006-inch air gap. Windings N1, N2, and N3 are wound around core number 1. During normal operation, the transformer flux is confined to core number 1. If one-half cycle unbalance occurs and core number 1 starts saturating, flux will start building up in core number 2, the zener diode CR5 will break down, and the voltage across L1 will increase, causing L1 to saturate sooner, resulting in faster turn-off of the conducting transistor. The zener diode is necessary to prevent winding N4 from loading winding N3 during normal operation.

An improved version of this approach is a circuit in which winding N4 is connected in series with winding N3. This circuit eliminates the zener diode and makes winding N4 more effective. A one-half cycle unbalance condition was created by inserting a resistance in series with one side of the output transformer. With the one-half cycle unbalance correction circuit connected as described, the unbalance condition disappeared. Further investigation of this approach showed considerable losses in the power transformer, resulting in low inverter efficiency. Because high inverter efficiency is of prime importance, this approach was abandoned.

Two new design approaches were used for the 90-watt LIVC. Both approaches used secondary or load current feedback for LIVC transistor drive. One method uses a current transformer in the secondary or load side to provide drive current for the inverter transistors. This method was suggested by NASA* and it worked very well. Efficiency of the inverter was improved and the "double on" and "half cycle unbalance" problems were minimized. The suggestion and use of secondary current feedback resulted

* NASA Report No. X-716-68-49 by E. R. Pasciutti.

in design of a more simple circuit for the LIVC. This circuit is illustrated in Figure 8. It can be seen from Figure 8 that the secondary or load current must flow through the base emitter junctions of inverter transistors and, therefore, provides the drive for these transistors. The base emitter junctions are protected from the high secondary voltages by the output diodes.

This circuit is practical only when the power transformer turns ratio is close to the most efficient operating transistor current gain. In the case of the battery LIVC, the transformer turns ratio is 31, and the most efficient operating current gain for the LIVC transistors is 30. The battery LIVC was first operated with the circuit shown in A, Figure 8. The circuit operated satisfactorily at a frequency of about 650 Hertz. The efficiency was about 76 percent. The LIVC was then operated with the circuit configuration shown in B, Figure 8. The LIVC worked very well, with an efficiency near 90 percent at the midload range. The final configuration for this LIVC is shown in Figure 9. It became necessary to place a small value resistor in series with base-emitter feedback windings. When the LIVC was operated, an excessive "double off" condition existed. Investigation showed that load current continued after the LIVC transistors turned off. There are three paths in the transistor circuits for this load current. One is the base-emitter junction of the transistor, another is the resistor across this junction, and the other is the transformer winding across this junction. Apparently, the current is not flowing through the base-emitter junction because the transistor is off at this time. The resistor across this junction has a high enough value (8.2 ohms) to limit the current flow much more than it actually is limited; therefore, the current must be flowing through the transformer winding across the base-emitter junction. This winding must present a very low impedance at this time for this condition to exist, and careful analysis shows this to be the case.

The probable explanation of what occurs is as follows: Assume that transistor Q1 (Figure 9) has just turned off. The direction of the current in the feedback winding and load current is as indicated by the arrows. Transformer

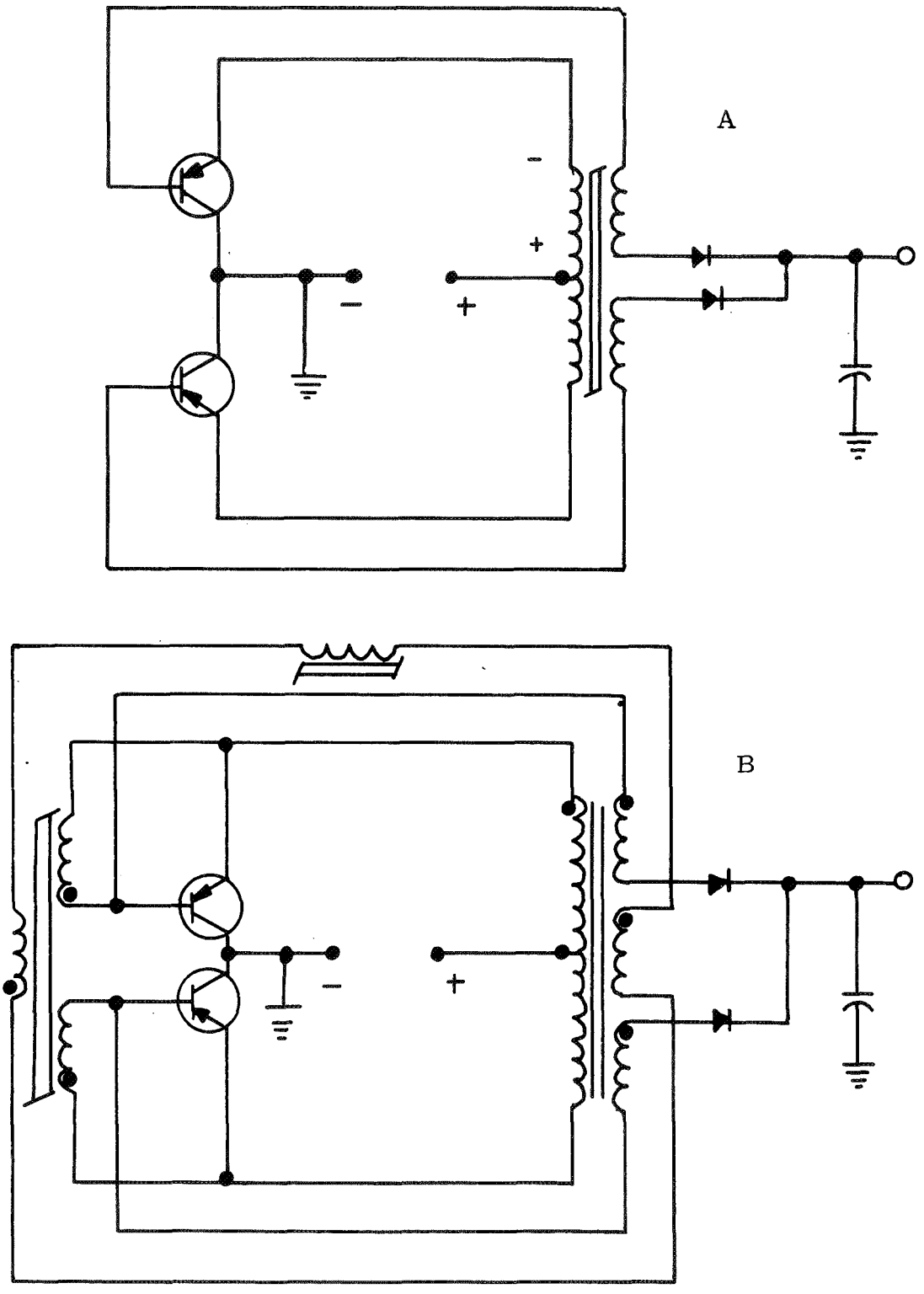


Figure 8. LIVC Using Load Current for Transistor Drive

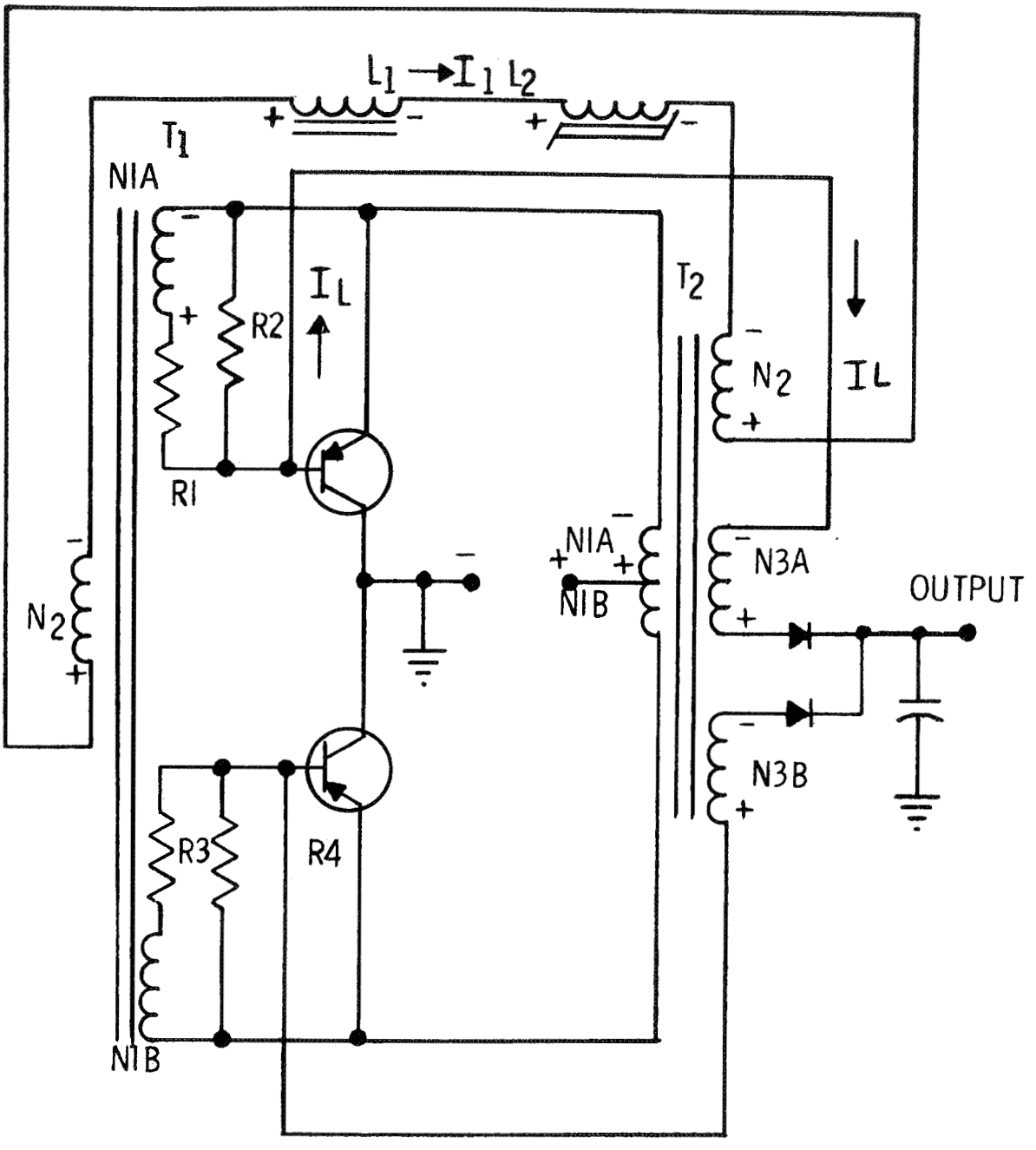


Figure 9. Battery LIVC Circuit

voltage polarities are for conditions just before turnoff. Choke L2 is saturated, the feedback voltage has dropped to zero, and the voltage across L1 has reversed to maintain its current in the same direction. This reflects back to N1A of T1 as a very low impedance when a voltage of the proper polarity is applied across N1A of T1. The voltage developed by the energy stored in N1A and N3A of transformer T2 is of the proper polarity and the load current will continue flowing through the low impedance presented by N1A of T1 until the energy in T2 is dissipated. Voltage developed across N1A of T1 at this time is in a direction to turn Q1 on again, but it is not large enough to do so. A one-ohm resistor was placed in series with N1A and N1B of T1 to limit the current and decrease the L/R time constant of that portion of the circuit, and the "double off" condition disappeared.

b. 60-Watt LIVC – The initial design for this LIVC is one used in a previous contract (NAS-5-10148). This circuit is shown in Figure 10. The method of current sensing for turnoff of the starting oscillator was changed. The original circuit sensed current in a separate transformer in the output. The modified circuit senses current from an extra winding on the power transistor base drive transformer. This change is shown in Figure 11. The circuit was breadboarded and tested. The initial circuit had a low efficiency, approximately 82 percent. A deltamax core was used in the power transformer in the initial design. The high maximum flux density of deltamax allowed use of a smaller core, thus reducing the volume of the circuit. It appeared that the low efficiency was due to excessive core loss, so a new transformer was wound and a supermalloy core used. When this transformer was used, the LIVC efficiency was over 90 percent. The final basic inverter configuration is that shown in Figure 8B. The efficiency was improved about 0.5 percent. Other than the slight increase in efficiency, the only improvement was elimination of the high current winding in the transistor emitter circuit. The possibility of a "double on" or "half cycle unbalance" problem was also minimized; however, these problems are not significant in this circuit.

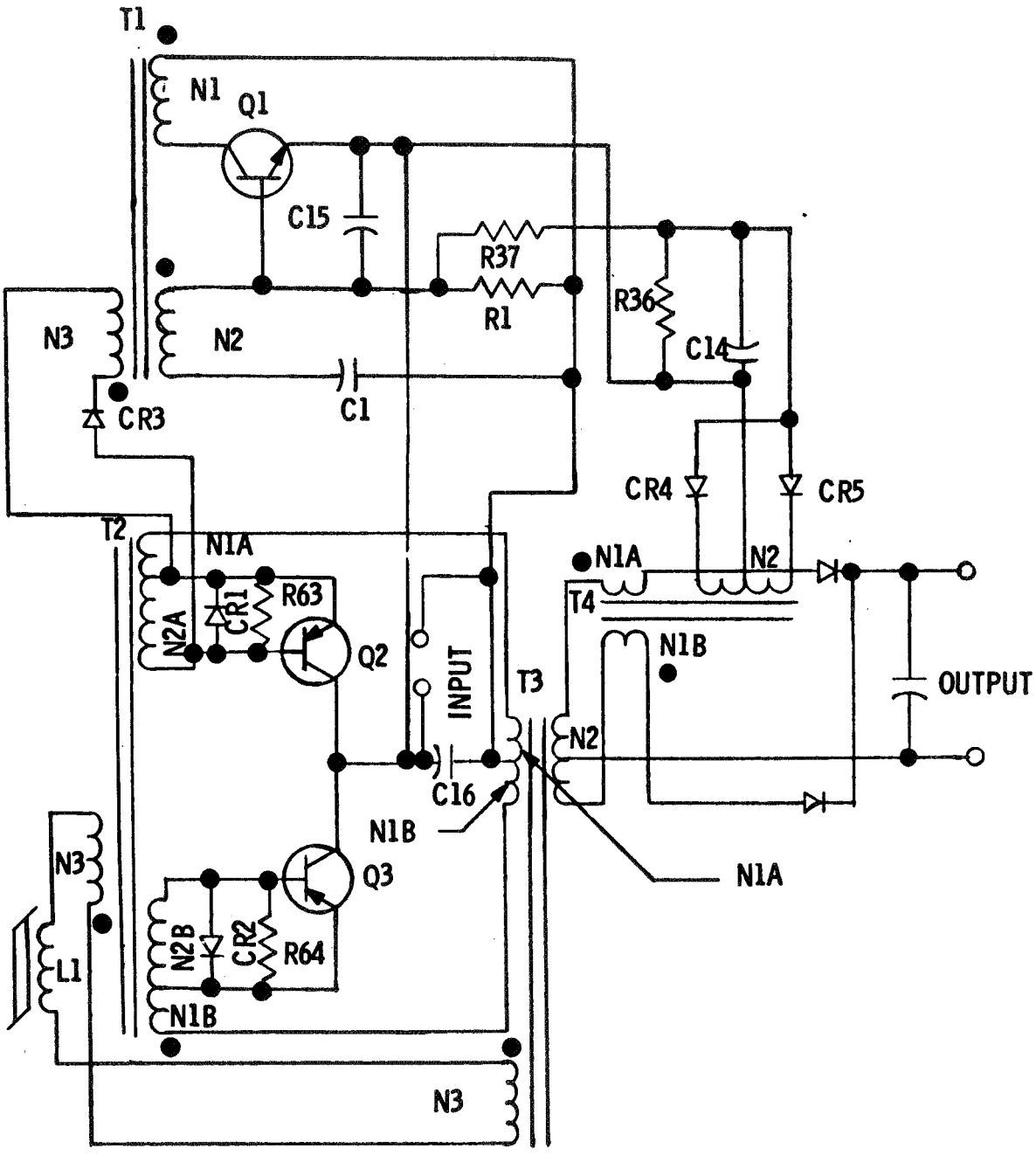


Figure 10. RTG LIVC with Current Sensing in Output Line

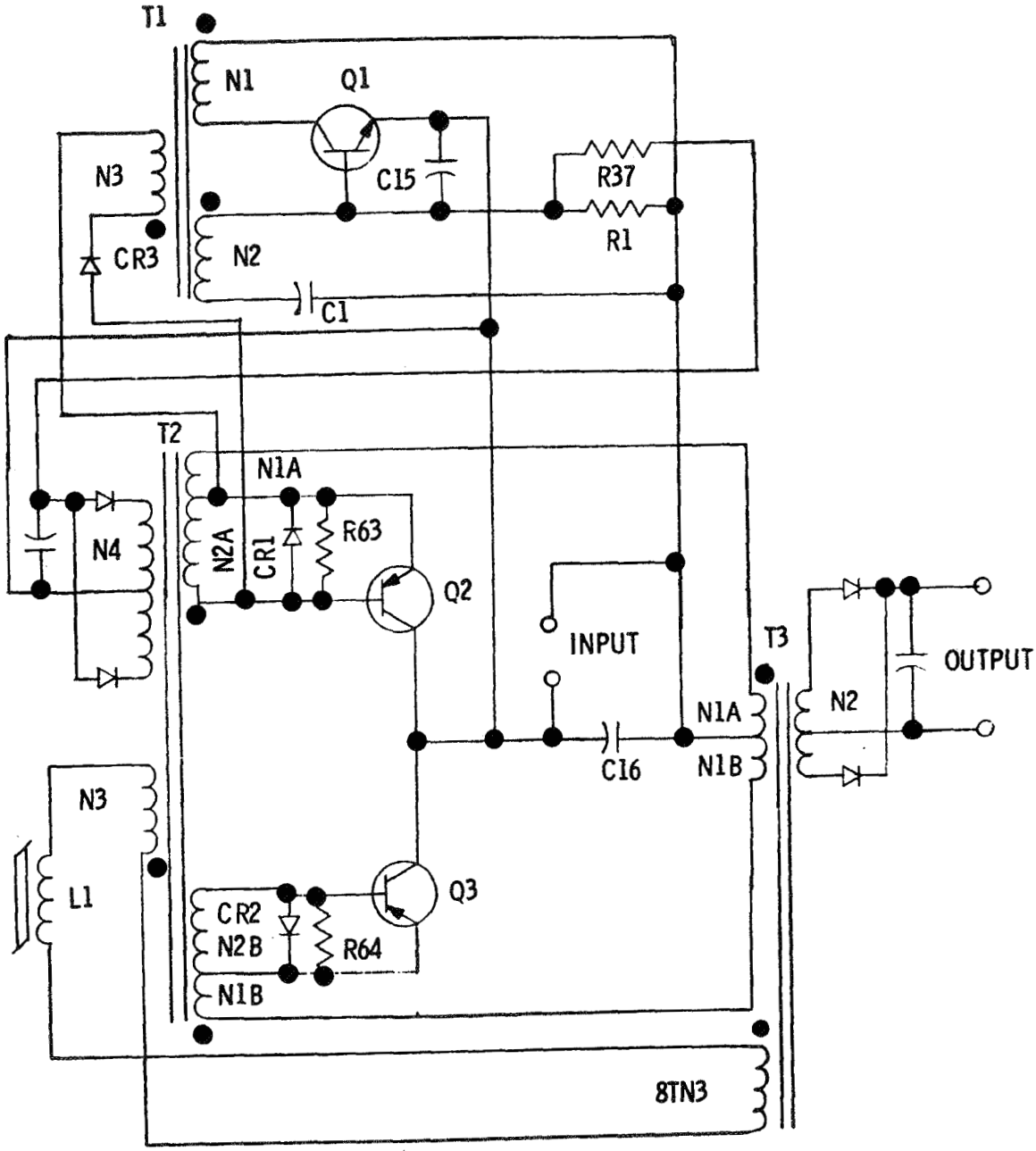


Figure 11. RTG LIVC with Current Sensing in Drive Circuit

A starting circuit using an SCR was designed and incorporated into both inverter circuits. Figure 12 shows three basic starting circuits. Only one transistor of one side of the inverter is shown. The winding used to develop voltage for maintaining the SCR off after the inverter has started can be from a current transformer or voltage transformer. Operation of the SCR starting circuit shown in Figure 12A is as follows: When power is applied to the inverter, gating current flows through resistor R3 and gates the SCR. When the SCR turns on, base current flows in the transistor and turns it on. The transistor will turn on hard through the normal regenerative action of the inverter. This causes the transistor to saturate; this back-biases the SCR and turns it off. Voltage is developed across the transformer winding and is applied to the gate in the proper polarity to keep the SCR turned off. An SCR is practical in this application because of the availability of SCR's with extremely high current gain. These can be maintained in an off condition with negligible power drain from the inverter when the inverter is running.

Figure 12B shows another version of an SCR starting circuit. This is the first circuit used in the 60-watt LIVC. In this circuit, base current for the inverter transistor is drawn through C1 when the SCR is gated. The resistor R1 has a large value. The value of resistor R1 has to be large enough to limit the SCR anode current to a point below the SCR holding current when C1 has charged. The purpose of this configuration is to ensure turnoff of the SCR. For some reason, the circuit shown in Figure 12B would periodically "hang up"; that is, the SCR would turn on and stay on and the inverter would not start.

The circuit shown in Figure 12C is the one used in the 90-watt LIVC. This circuit is used because the power transformer output winding was used for the "off" maintaining voltage. This voltage is relatively large, and power loss in maintaining the SCR off could be significant, but a much larger value of R4 can be used when the transistor is added. The circuit in Figure 12C can be made to oscillate until the inverter is free-running. When the SCR

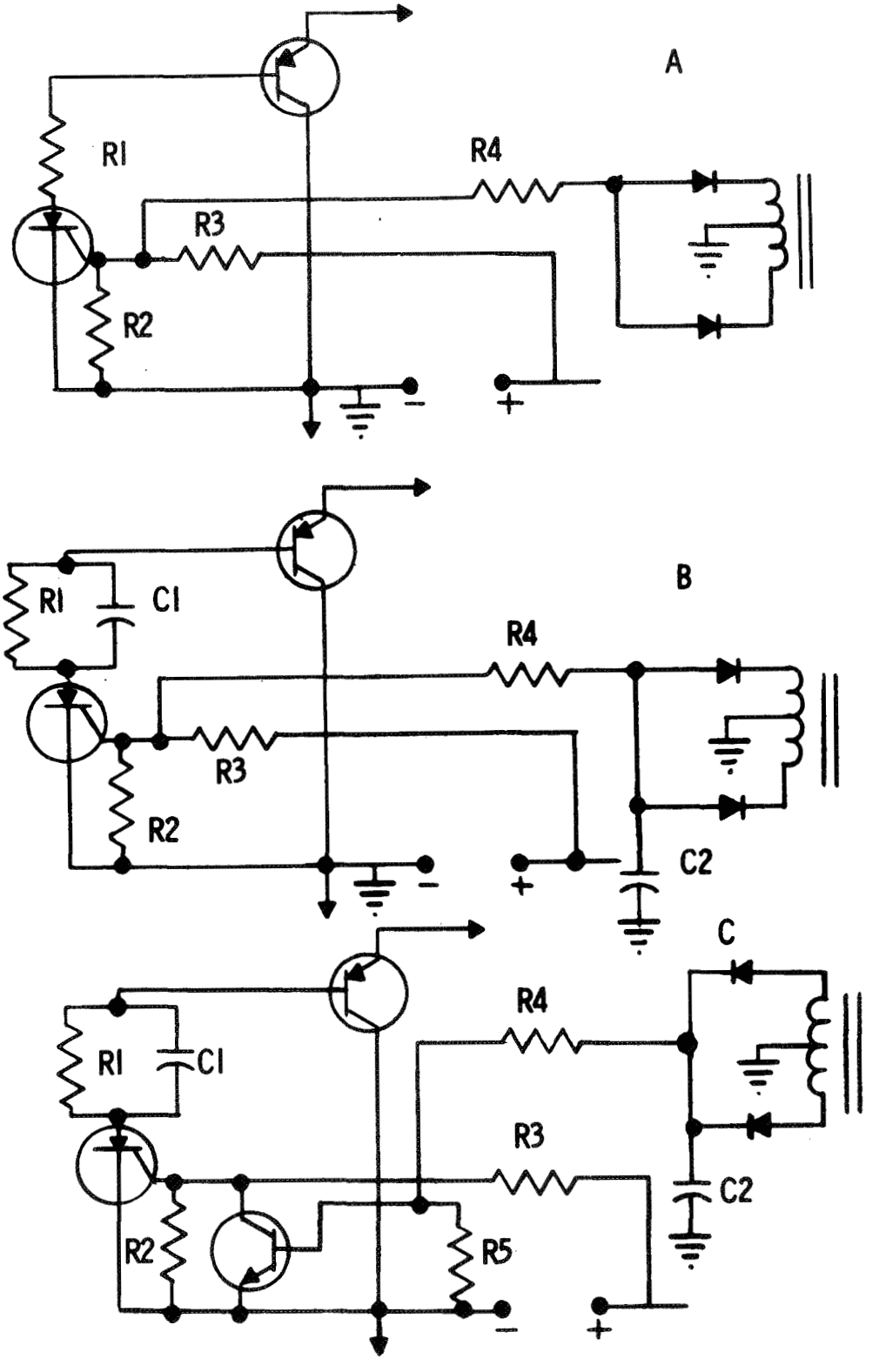


Figure 12. Inverter SCR Starting Circuits

turns on, it turns on one side of the inverter. This develops a voltage on C2 and applies a turnoff voltage to the starting circuit. The time constant of R4 and C2 is made large enough to allow C1 to discharge through R1. If the inverter does not start, C2 will discharge through R4, the "hold off" voltage will drop to a low enough value, and the SCR will turn on again and try to start the inverter. This process will continue until the inverter starts or the input voltage is removed.

It may be possible to make the circuit in Figure 12B oscillate, but the value of R4 is limited to a relatively low value. This means that in order to get a long enough time constant for C1 to discharge, the value of C2 must be made much larger. If the value of C2 is made much larger its charge time will be too long and the "hold off" voltage will not be large enough before the inverter first half cycle is completed. Figure 13 shows the 60-watt LIVC with the original starting circuit and with an SCR starting circuit.

One potential problem with this circuit is that the forward voltage of an SCR is relatively large, on the order of 1 volt. This may create problems in the battery LIVC at cold temperatures when the SCR forward voltage is higher, and the battery impedance may be higher. The 60-watt LIVC starting circuit was modified to be a self-oscillating type like the one used in the battery LIVC. The inverter would always start when power was applied; however, occasionally the inverter would stop oscillating when the overload circuit was checked and the output switching transistor turned off. Apparently, under certain conditions, the time of current interruption before one of the overvoltage SCR's conducted was sufficient to cause the inverter to stop oscillating. Once it stopped it would not restart. Addition of the self-oscillating starting circuit has eliminated this problem.

c. Computer Program – A computer program has been developed to determine optimum turns ratios of the LIVC power transformers for the most efficient load sharing of the two LIVC's. If the two LIVC's operated with 100 percent efficiency, the problem of calculating these turns ratios would be

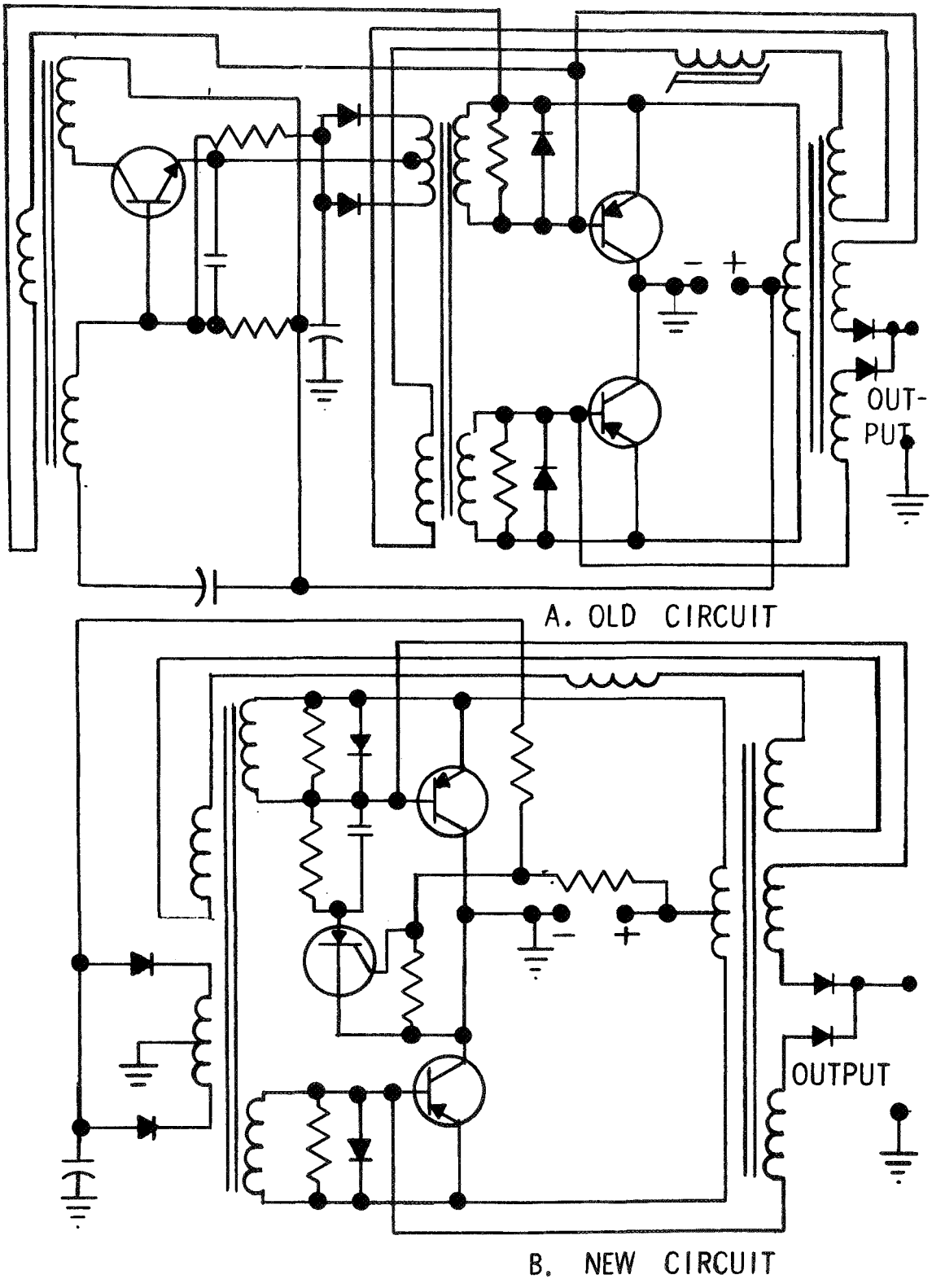


Figure 13. RTG LIVC with Different Starting Circuits

quite simple; however, the LIVC's do not operate at 100 percent efficiency and the losses in each LIVC result in voltage drops in the output which affects the load sharing of the two inverters. The equivalent circuits, development of equations for the computer programs, the computer programs, and computer output for a given set of conditions are shown in Appendix I.

The equivalent circuit for developing the program equations was kept as simple as possible. This was done to expedite initial development of the programs. All of the losses of each inverter are represented by one resistor in each inverter section. This may not seem legitimate because much of the loss in each inverter is caused by nonlinear devices such as diode junctions and core losses. However, all the calculations were made at one power level, and the total system losses will not change significantly under these conditions. If the program is modified to vary the power output, it would be necessary to develop a more exact circuit model. This program does not include the regulator circuit. It is assumed that the regulator efficiency is 90 percent which results in 150 watts at the input of the regulator for 135 watts on the output.

One of the problems with this program is that it is either necessary to know or assume the efficiencies of the two inverters. In this case the efficiencies were measured on the existing breadboard. Other parameters that must be known or assumed are the voltages and impedances of the power sources, and these parameters are usually known.

This computer program actually consists of two programs. The initial program VIC was developed to determine the values of the resistances that represent the losses in each inverter for given efficiencies. The program WOL was developed to calculate input currents for various turns ratios in each inverter. The program VIC was modified to include WOL by calling it in as a subprogram. The program is written so that any value of input power source voltages and impedance can be used. As the program now

stands, the final calculations and outputs are given for a load of 150 watts. This can be changed easily by a slight modification in the program.

Referring to the print-out shown on page I-4 of Appendix I, I2, I3, EO, N1, P, and RO are the RTG current, battery current, output voltage, battery LIVC output transformer turns ratio, power output, and load resistance (at 150 watts power output), respectively. I2 and I3 are in amperes X10-2 and must be multiplied by 100 to get the correct value. EO is in volts X10-2 and must be multiplied by 100 to get the correct value. P is in watts X10-3 and must be multiplied by 1,000 to get the correct value. RO is in ohms.

For some unknown reason, the computer prints out for one more value of N1 than is required, but it repeats the information for the previous value. It can be seen that for any given value of N the RTG current decreases as the value of N1 increases. This is to be expected because the battery LIVC will supply more of the load current as its output voltage goes up. It is somewhat surprising, however, to see that the battery current also decreases as N1 is increased. This indicates the whole system operates more efficiently with higher voltage outputs from the battery LIVC. The print-out also shows that the RTG current increases and the battery current decreases as the RTG LIVC output transformer turns ratio is increased. This is what would normally be expected. There does not seem to be a point of optimum balance where the battery current hits a minimum value. The breadboard showed the same trends indicated by the computer when the turns ratios were actually varied slightly on both transformers. The only difference was that the RTG current at maximum load stayed very close to 22 amperes.

It may be that this program will not have any actual value in determining optimum operating points. It may be that the optimum parameters occur at some impractical value. There is a limitation on the output voltage because of component ratings and a physical limitation on the number of turns that can be put on the cores. The program does have moderate value

in that turns ratios, output voltage, and power source currents can be calculated for any two sets of power sources. The voltages and impedance of the power sources must be known, and the efficiencies of the inverters must be known or estimated. The program can be modified for any power output level.

d. Overvoltage Protection Circuit – A zener diode-controlled SCR overvoltage protection circuit has been considered for this application. This circuit will prevent dangerous unloading of the RTG and prevent excessive temperatures at the RTG hot junctions if the power conditioner is unloaded. Overvoltage is prevented by loading the LIV converter and RTG when the zener-controlled SCR's are gated into conduction. The RTG characteristic ("Peltier Cooling") under load prevent excessive hot junction temperatures in the RTG. This circuit was initially developed by NASA/GSFC and has been incorporated into the breadboard converter with automatic failure-sensing and automatic failure compensation under contract NAS-5-10148. It was also incorporated into the dual redundant converter for the Nimbus B satellite application under contract NAS-5-10269.

An overvoltage circuit of this type was connected to the output of the 60-watt LIVC and the load decreased to allow the RTG voltage to go up and initiate the overvoltage circuit. A problem was encountered when this circuit was initiated. When one of the SCR's conducts and shorts out the output, the RTG output voltage is reduced to near zero. Essentially, this removes the normal frequency-determining device from the circuit because this circuit is voltage-sensitive. During this condition, the frequency-determining device is the power transistor current drive transformer. With the original design the on pulse became very long, which resulted in a large "notch" in the output voltage to the regulator. The regulator was able to handle this and maintain the D. C. output voltage to within the specifications; however, the ripple content of the output increased to over 200 millivolts peak-to-peak. There are several ways to minimize this problem. One is to increase the value of the capacitors on the input and output of the regulator.

This is undesirable because it increases the size and weight of the system. Another solution is to redesign the current transformer so that it will saturate faster when the overvoltage circuit operates.

The voltage on the primary of the current transformer (which will be the voltage that determines the saturation time) is that which is seen on the secondary, divided by the turns ratio of the secondary to primary. This turns ratio is 10:1 and is determined by the most efficient drive for the transistors being used. The base voltage at 6 amperes base current (60 amperes collector current) is 0.7 volt. This voltage reflects to the primary as 0.07 volt. With this voltage on the primary, the saturation time of the core is approximately 0.5 millisecond. It is possible to decrease this time by using a core with a smaller cross-sectional area, reducing the number of turns, or a combination of both. Reducing the number of primary turns to 1 (two primary turns are being used now) will double the magnetizing current (IM=2Hc7). This should be insignificant because the magnetizing current is less than 0.1 ampere (assuming Hc=0.01 oersted).

Another solution to the problem is to use a modified circuit for the overvoltage protection. The schematic for this circuit is shown in Figure 14. This circuit works the same as the previous circuit except that when one of the SCR's switches on, current is drawn only for the portion of time required to charge the capacitor. When the capacitor nears full charge the charging current will drop below the holding current of the SCR and SCR will turn off. The capacitor can be sized to get the desired voltage limiting with shorter low-voltage pulses.

A more simple approach is shown in Figure 15. It can be seen from Figure 15 that the circuit still uses SCR's as the switching elements and a capacitor in series with the SCR to limit the "on time" of each SCR. When the RTG LIVC secondary voltage exceeds the zener breakdown voltage, one SCR is gated. The SCR stays on and draws current until the capacitor is charged or the voltage reverses; the other SCR turns on and charges the capacitor

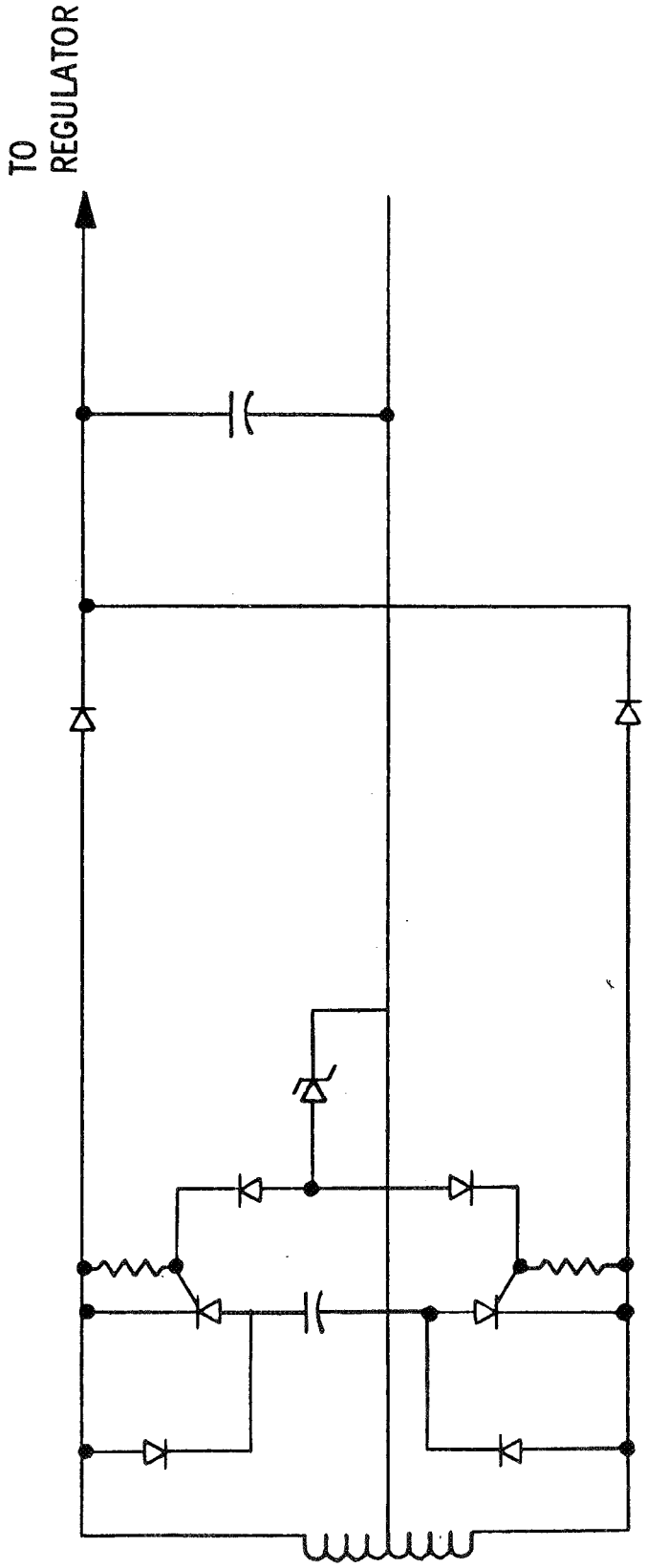


Figure 14. Modified Overvoltage Protection Circuit

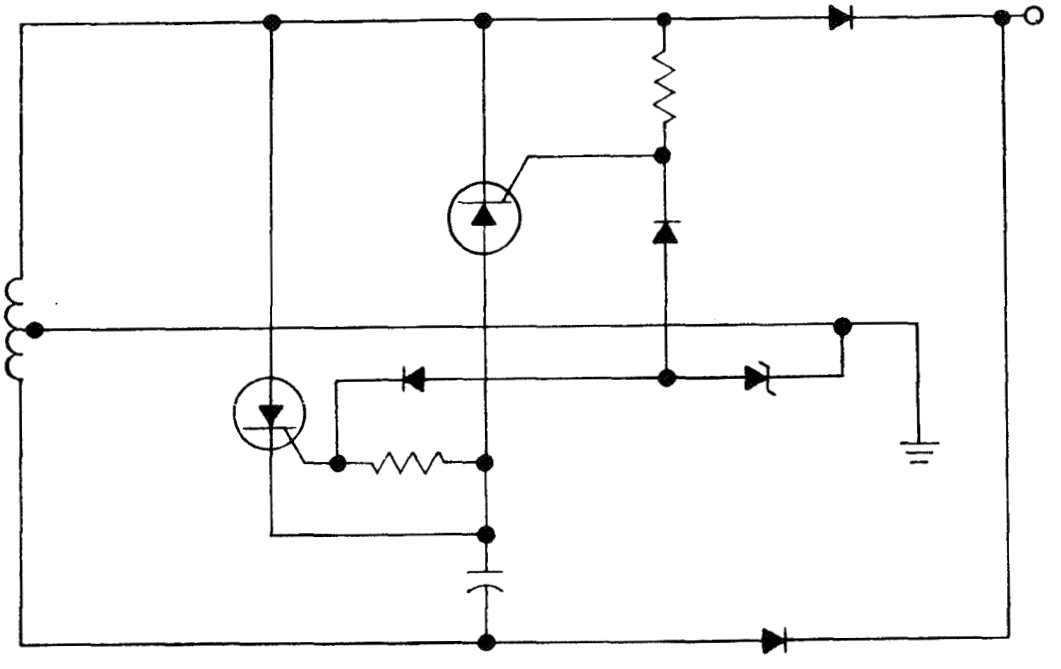
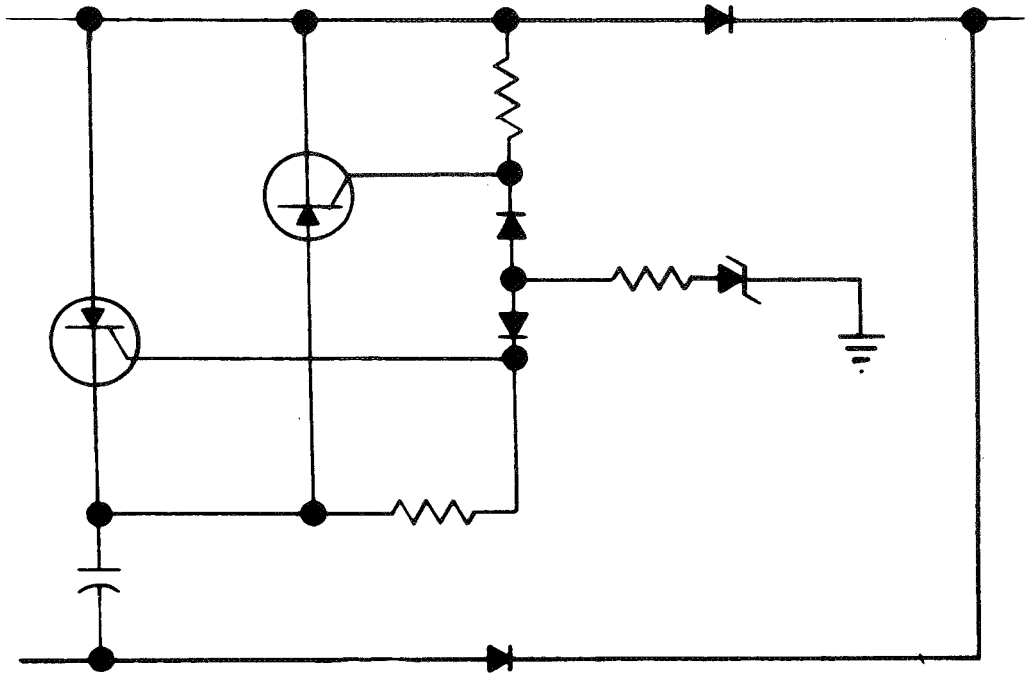
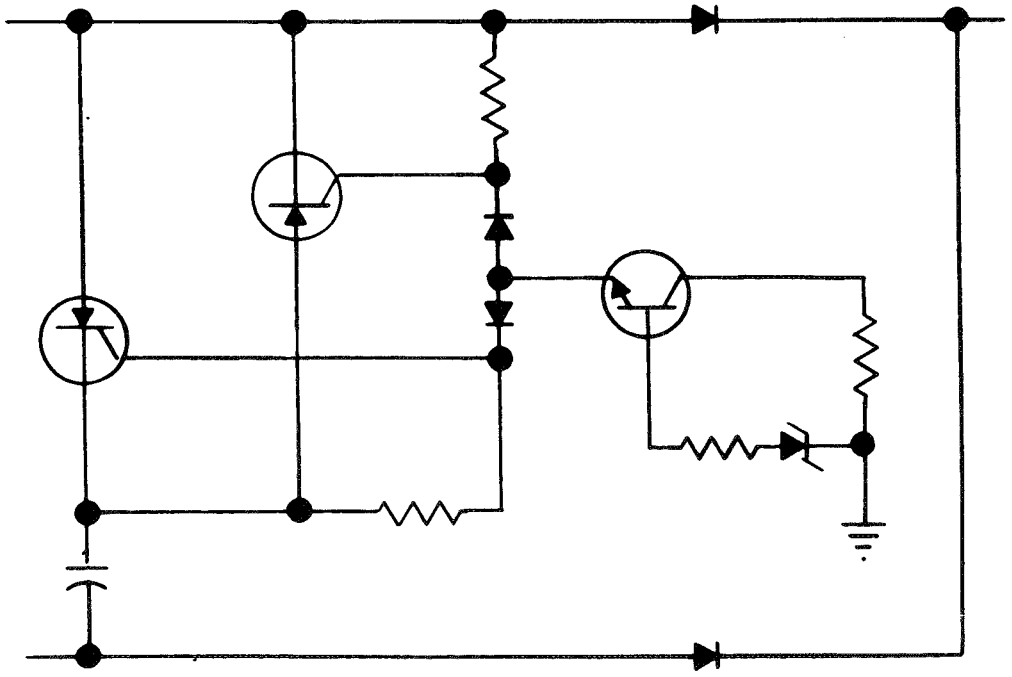


Figure 15. Overvoltage Protection Circuit

in the opposite direction. The capacitor is sized so that, together with the input resistance, the RC time constant limits the SCR "on time" to a minimum value, thereby preventing transformer core saturation and minimizing output ripple during overvoltage condition. Several modifications were made to this circuit. The first modification is shown in Figure 16. A transistor was added to the SCR gate circuits to ensure firing when the inverter output voltage was close to the zener breakdown voltage. The variation in gate breakdown voltage and gate current required to fire is such that the RTG voltage limiting could vary considerably with temperature. If the 1,000-ohm resistor in series with the zener were lowered in value or removed, the variation due to changes in gate current required to fire would be minimized. However, this resistance value must be kept large enough to limit the gate current to prevent gate burnout. It is possible to get fairly high voltage spikes before the SCR turns on and these high voltage spikes could produce destructive gate currents if the resistor value was too low. With just the resistor and zener diode in the circuit, the RTG voltage was limited to about 4.8 volts. Use of the same zener diode with the transistor resulted in RTG voltage limiting to about 4 volts. Further circuit modifications are shown in Figure 17. One of the changes was to add a .01-uf bypass capacitor from the gate to cathode of each SCR. There was some intermittent firing of the SCR's and these capacitors eliminate this problem. A .01-uf capacitor was added from ground to the base of Q10 to assure the overvoltage circuit SCR turns on when the simulated RTG voltage is applied to the RTG LIVC. Turnon of the regulator is delayed for 3 seconds (because of the 3-second delay circuit when overload occurs), and the only significant load on the RTG LIVC is the overvoltage circuit and the charging load of the filter capacitor at the input of the regulator. At initial turnon, the RTG LIVC will turn on, charge the filter capacitor, and then turn off. The overvoltage SCR's do not turn on. Addition of the capacitor causes the overvoltage circuit to operate and keep the RTG LIVC operating until the regulator circuit turns on.



A. OLD CIRCUIT



B. NEW CIRCUIT

Figure 16. Overvoltage Protection Circuit

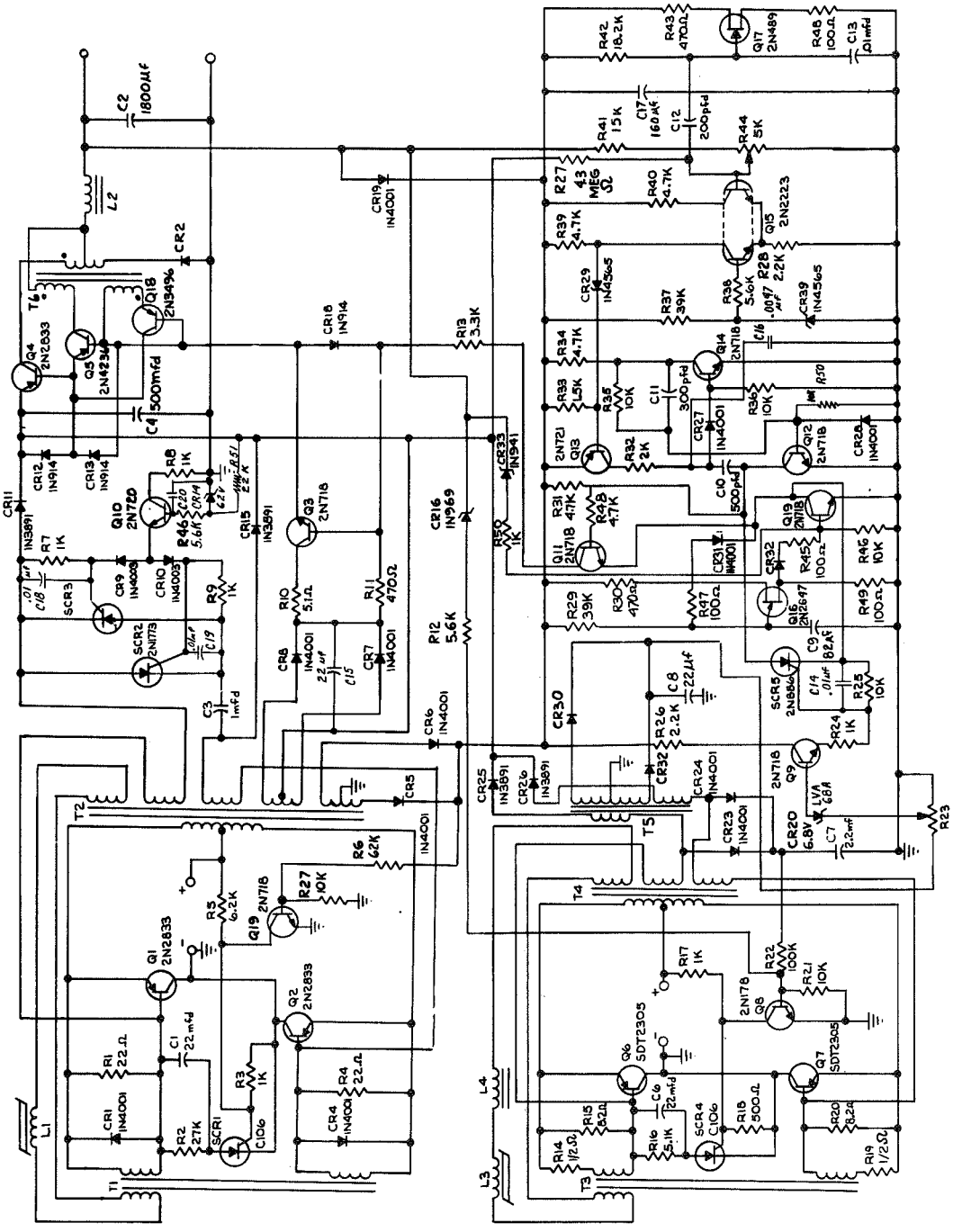


Figure 17. LIVC and Output Regulator Circuits

A resistor was connected from the junction of R46 and CR14 to the inverter D.C. output. This resistor provides a bias on the zener circuit in the overvoltage circuit and a method for calibrating the voltage at which the RTG is limited. A potentiometer could be used here, but using a selected resistor appears more practical. Further investigation showed that the overvoltage circuit was more stable with the new modification and with the transistor removed. The final circuit configuration for the overvoltage protection circuit is shown in Figure 18.

e. Pulse Width-Modulation (PWM) Voltage Regulator – The combined output power from the two potential sources of energy, either directly from the RTG through the 60-watt LIVC or from the silver-zinc battery through the 90-watt LIVC, will be applied to a PWM voltage regulator. The pulse width-modulation voltage regulator will be very similar to that delivered to NASA/GSFC under contract NAS-5-10148, in that the previous regulator also operated from a summation of more than one LIVC output. The schematic for the initial design of the voltage regulator is shown in Figure 19. There is one major and important difference in this design. The previous designs accomplished variable pulse widths by D. C. -modulating the sawtooth wave derived from a unijunction relaxation oscillator. In the present regulator a unijunction oscillator is used to initiate a monostable multivibrator. The pulse width of a monostable multivibrator is usually governed by an RC network in the base circuit of the normally on transistor. In this circuit the pulse width of the multivibrator is varied by the output of a differential amplifier. The differential amplifier senses variations in the output voltage. The frequency of the pulses is determined by the unijunction oscillator and the on (or off) time is determined by the pulse width from the monostable multivibrator. This circuit has excellent stability and can be operated at a very high gain. The original circuit, with no attempt to adjust the system gain, was able to maintain the output voltage at 28 volts ± .02 percent. The frequency of the unijunction oscillator could be changed from 7 KHz to 14 KHz with no change in the output. The circuit will probably be adjusted to operate at a lower gain to simplify temperature compensation.

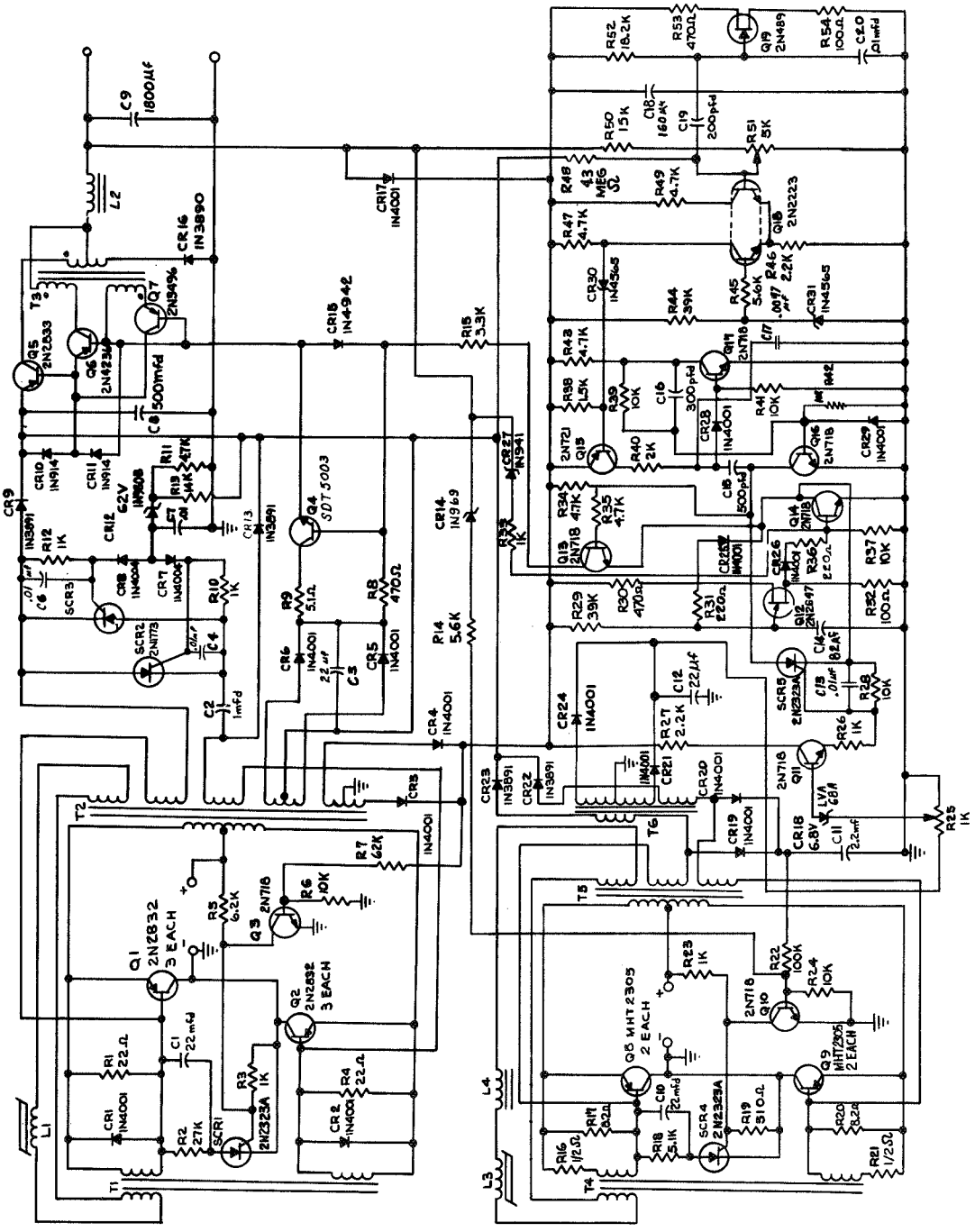


Figure 18. Final Configuration of LIVC and Output Regulator Circuits

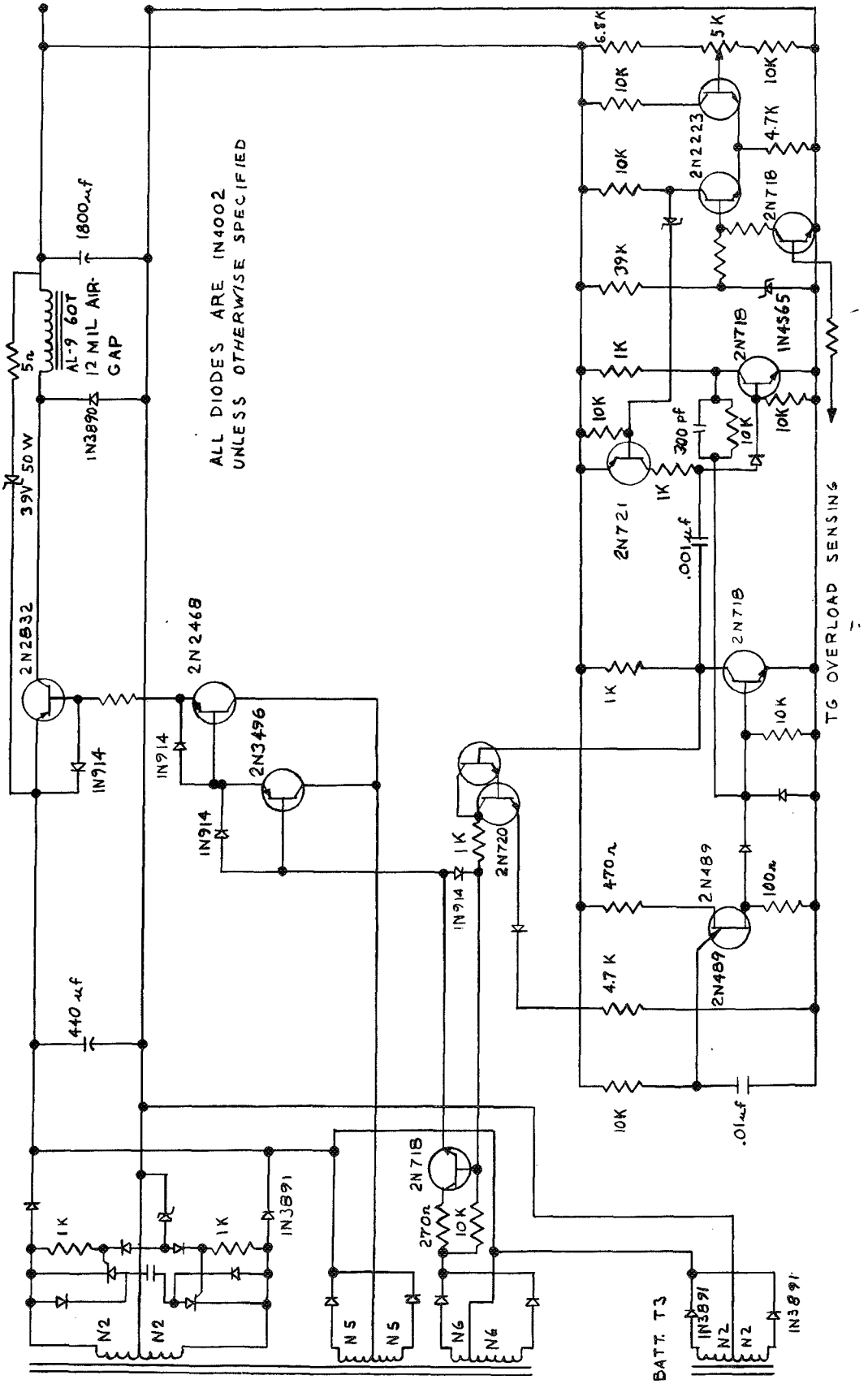


Figure 19. Output Voltage Regulator

No effort has been made to determine the amount of temperature compensation that will be needed. A zener diode is connected across the line switching transistor to supply voltage to the regulator on start. The breakdown voltage of this zener diode is such that it will not conduct when the output voltage comes up to 28 volts. A resistor is placed in series with this diode to limit the current and power dissipation under overload conditions.

In an effort to improve the efficiency of the regulator the line switch was changed to a Darlington configuration. This improved the efficiency slightly. The efficiency of the regulator was about 91 percent at this time. The next modification was also in this portion of the circuit.

This modification consisted of addition of a current transformer for obtaining drive for the output switching transistors. This circuit is shown separately in Figure 20. The current drive for transistors Q4 and Q5 (Figure 20) is obtained from the secondary windings of the current transformer and these secondary currents are proportional to the load current. The current transformer core is reset by the free-wheeling current flowing through the free-wheeling diode CR2 when the power switching transistor turns off. The high secondary impedances for the transformer polarity during reset result in a high voltage reflected on the primary and a very short reset time. This circuit results in faster switching and about a 2 percent increase in efficiency at maximum load. The increase in efficiency at lower loads should be greater because the fixed losses in the output switching circuits are less.

The zener diode and resistor network used for supplying voltage to the regulator for starting was eliminated by supplying an auxiliary power source from the RTG LIVC power output transformer. The voltage from this source is never greater than about 23 volts and does not supply power during normal operation. The normal power for the regulator is from the 28 volts through a diode. The purpose of the diode is to isolate the auxiliary power source from the output during overload conditions or any other time that the 28 volts is not present on the output. The final configuration of this circuit is shown in Figure 18.

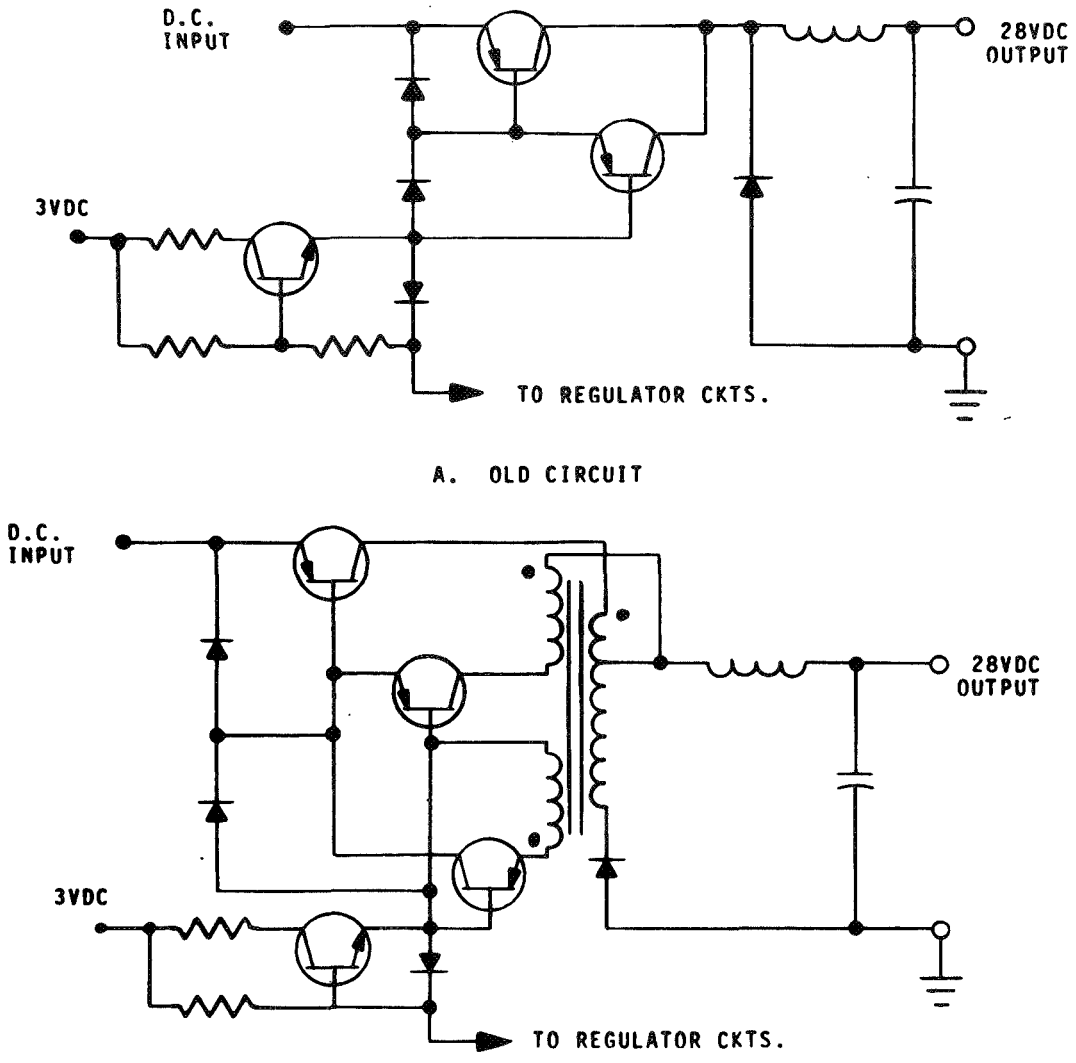


Figure 20. Output Switching Circuits

f. Current Limiter – The initial method considered for current limiting or overload protection was to use a magnetic amplifier in the output. One winding of the mag-amp transformer would be connected in series with the output. When the D. C. current through this winding reached a certain value the transformer core would saturate, decreasing the high A. C. impedance in other windings of the mag. amp., and allowing an A. C. signal to pass and be used to turn off the output regulator. After further consideration it was felt that a more simple approach would be to use a current transformer to sense current in the battery LIVC.

Using a winding on the LIVC current drive transformer to provide the overload signal is by far the simplest approach for overload current sensing. However, the voltage change on this winding depends on the voltage change in the loaded secondary (base drive circuit). As the current in the primary winding increases, the current in the base drive circuit increases. The voltage change in the base drive follows the forward voltage characteristics of the base to emitter junction of the transistor. A curve of these characteristics is shown in Figure 21. The figure indicates that a considerable change can occur in current with very little change in the voltage. This would require a very sensitive and accurate sensing circuit for the overload sensing. The change of voltage with current could be increased by putting a small resistor in series with the transistor bases. This reduces the efficiency of the system because of the added losses in the resistors.

The first breadboard current limiter design is shown in Figure 22. The portion of the circuit within the dotted line is the overload circuit. The circuit outside the dotted lines is the drive and series line switching portion of the output regulator.

Theory of operation of the overload circuit is as follows: A measure of the base voltage of the battery LIVC is obtained from the base transformer in this inverter. This voltage is proportional to load current. When this voltage gets high enough the zener breaks down and applies a signal to transis-

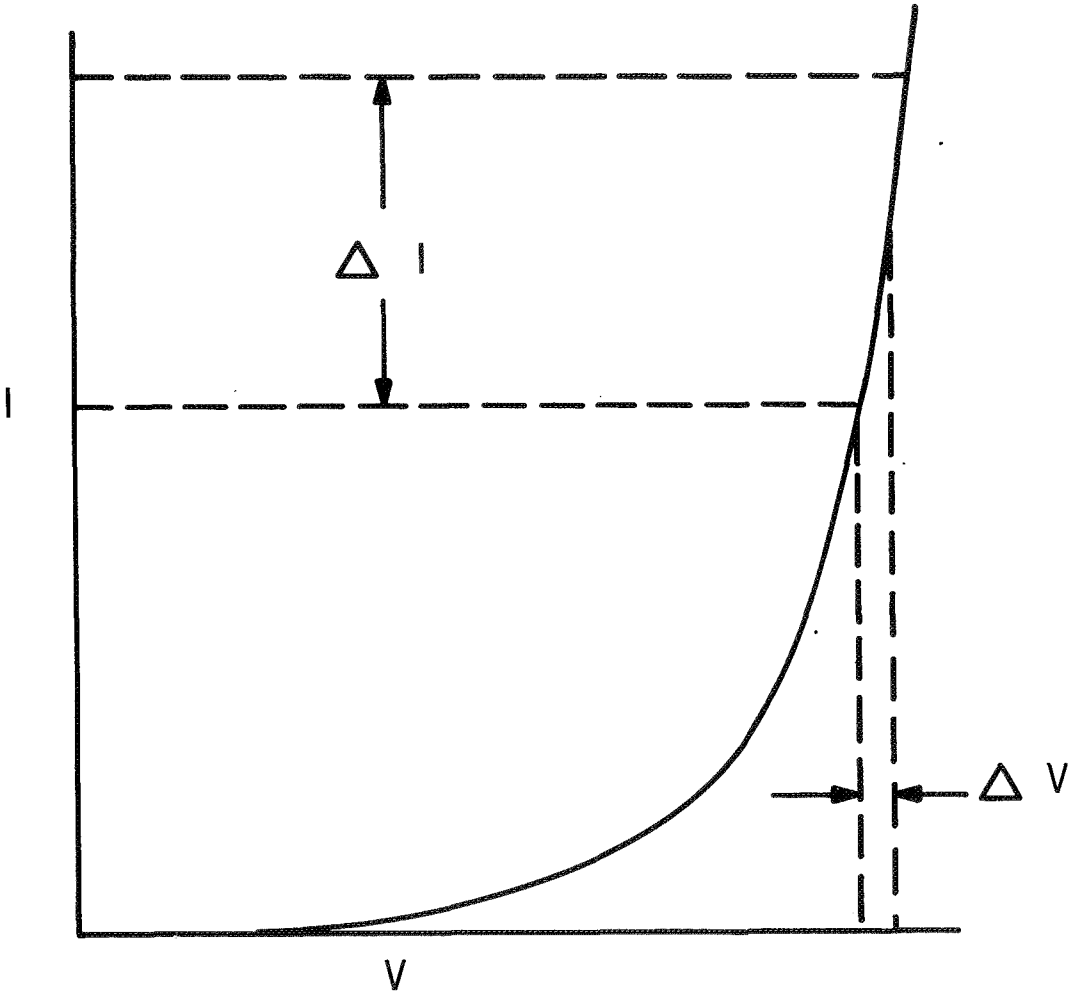


Figure 21. Forward Characteristics of Emitter to Base Junction

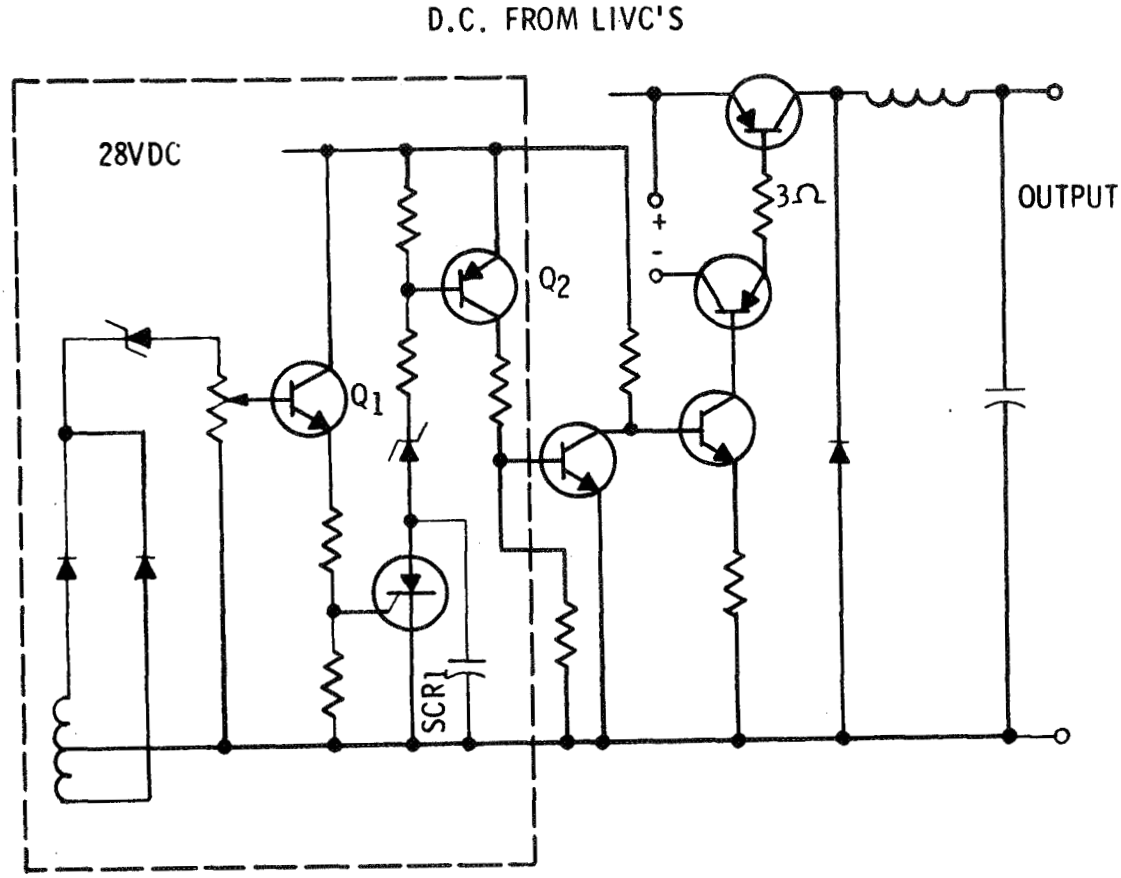


Figure 22. Overload Protection Circuit

tor Q1. The potentiometer is used for fine adjustment of the set point for maximum overload current. When transistor Q1 turns on, SCR1 is gated and turns on transistor Q2. Transistor Q2 turns on the transistor in the regulator that turns off the main series switching transistor in the output line. A zener is connected in series with SCR1 to ensure turnoff of the SCR when the 28 VDC decreases. This voltage is obtained from the output and will not drop completely to zero unless the overload is a short circuit. If this voltage does not drop to zero, the SCR may not turn off because the current through the SCR may not fall below the minimum holding current of the SCR. A capacitor is placed across the SCR to provide a low-impedance source for turnon of the SCR. If this low-impedance source is not present, the SCR acts like a linear amplifier when very small gate signals are present. The condition of very small gate signals does exist in the form of noise or spikes from the inverter base transformers. Without the capacitor across the SCR, the SCR responds to these spikes as a linear amplifier and turns on and off. This results in erratic switching near the overload turnoff point. A filter on the input to Q1 would also eliminate this problem; however, it creates another. The filter capacitor delays the overload signal and an abrupt overload could burn out the line switching transistor before "turnoff" occurs.

When the overload point is reached (approximately 95 amperes battery current), the main switching transistor turns off. When this transistor turns off, the battery LIVC turns off because of loss of sufficient inverter transistor drive current. The RTG LIVC will remain on because there is still some load current being drawn through the zener-resistor network around the main switching transistor. The output voltage drops from 28 VDC to about 3 VDC, and the output current drops from about 6 amperes to about 0.5 ampere. As the overload is increased, the output voltage will decrease to zero and the current will increase to about 1 ampere. These characteristics are shown in Figure 23.

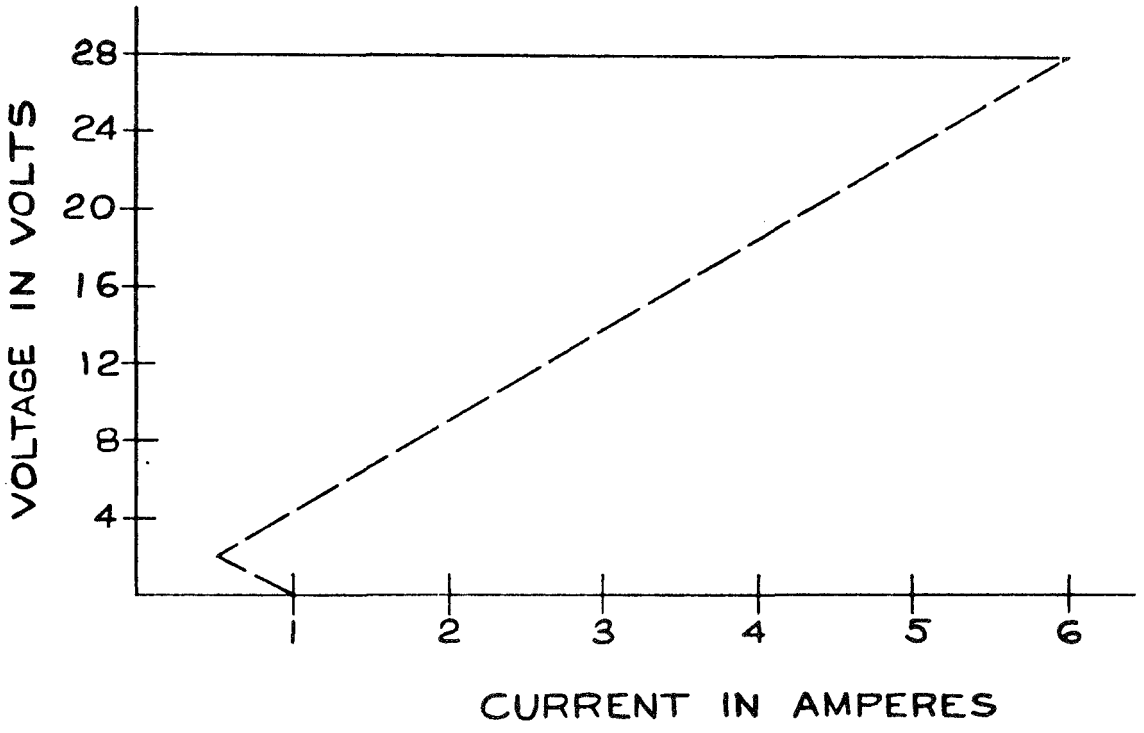


Figure 23. Regulator Output Voltage vs. Load

To prevent the system from attempting to turn on immediately because the main load source (the battery LIVC) has turned off and the overload signal source is removed, an overload reset circuit has been incorporated. The overload reset circuit consists of a transistor in series with the emitters of the voltage regulator differential detector (see Figure 24). This transistor receives its drive from the output voltage through a 4.7-volt zener. When an overload occurs, the output voltage drops below 4.7 volts, this transistor is turned off, the differential detector is removed from the circuit, and the main switching transistor will not turn on. If the overload is reduced to a point where the output exceeds 4.7 volts, the transistor turns on and the regulator becomes operational. The main switching transistor will turn on, the load current will increase sufficiently to sustain operation of the battery LIVC, and the system will start operating with 28 volts output. The load current will be about 5 amperes and the battery current will be about 85 amperes. The battery current at maximum specified load is about 70 amperes, so the 85 amperes will be an overload condition, but not a dangerous one. This overload circuit is somewhat complex, but it is necessarily so because of the peculiar, abrupt changes of input power sources during overload conditions.

One change was made in this current limiter circuit. In the original circuit a 23-volt zener diode was connected in series with the SCR in the current-limiting or overload detecting circuit. This was to ensure that the SCR would turn off when the output voltage dropped under overload conditions. It was necessary to connect a capacitor across the SCR to provide a low-impedance source to ensure fast and hard turnon of the SCR when an overload was sensed. In the modified circuit, SCR turnoff is accomplished by connecting the SCR to the voltage overload reset transistor collector. This transistor turns off when an overload is sensed. This connection eliminates the zener diode in the SCR anode circuit and the capacitor across the SCR. A small capacitor was connected from the gate to anode of the SCR to bypass gating signals from pickup or system noise.

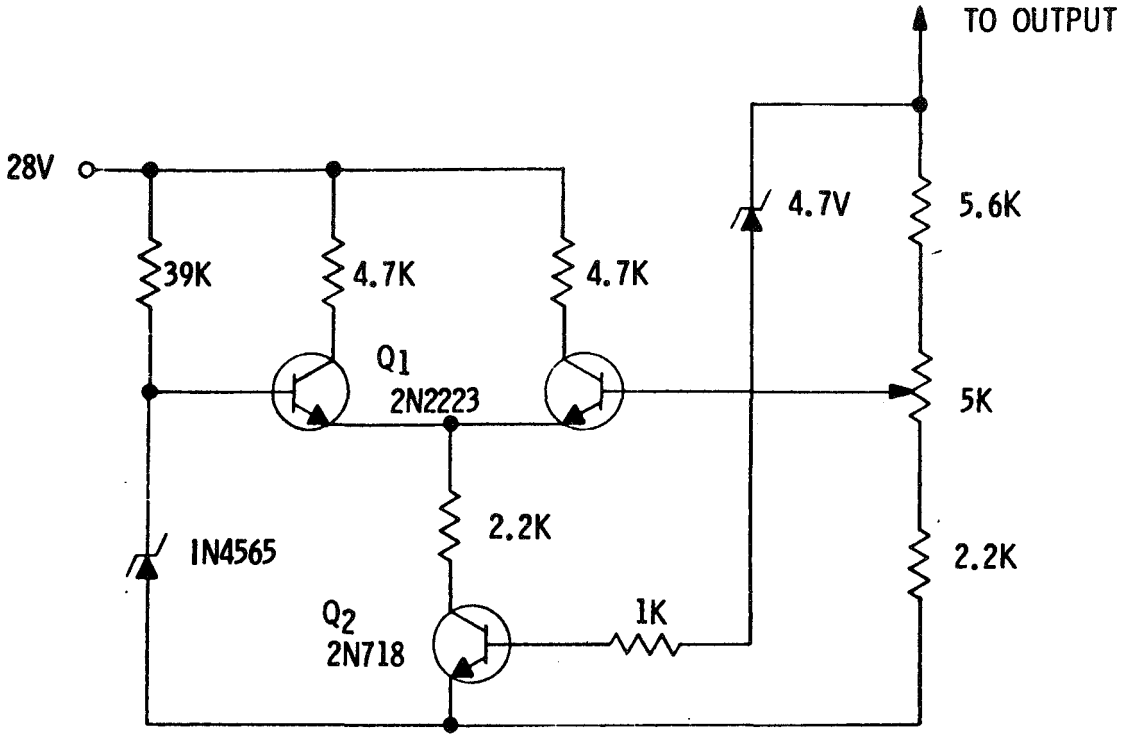


Figure 24. Voltage Overload Reset Circuit

It became necessary to make some major modifications in the overload protection circuit. When the overvoltage circuit was modified and operated at a lower RTG voltage it was found that the transients created affected the stability of the overload protection circuit. The switching was unstable right at the cutoff point and was also unstable when the load was reduced to a point below the overload condition, and the system tried to turn on again. The overvoltage circuit always operates during overload conditions because there is insufficient RTG current at this time to hold the RTG voltage down to its maximum allowable voltage.

The overload protection circuit consists of two separate circuits, the overload sensing and "turnoff" circuit and the overload removal sensing circuit. They are shown in Figures 25 and 26, respectively. The overload is sensed (Figure 25) and transistor Q1 is turned on. The SCR1 is gated and clamps the base of Q5 through a 4,700-ohm resistor to ground. This turns the power output switching transistor off. When the power output transistor turns off, the 28-volt output drops to zero and transistor Q2 turns off. This turns the SCR off and assures turnoff of Q5. In the original circuit, transistor Q5 was turning on intermittently during overload conditions because of transients appearing on the B+ for this circuit. With the new circuits, transistor Q5 and the power output transistor will stay off until the overload removal sensing circuit turns them on.

When the output voltage drops and transistor Q2 turns off, the unijunction relaxation oscillator shown in Figure 26 begins oscillating. The oscillating period is approximately 3 seconds. Every time the oscillator pulses, transistor Q2 turns on and the regulator operates. If the overload is still present it is sensed immediately and the system is again turned off and waits 3 seconds for another pulse. If the overload has been removed, the system will go back to normal operation. Transistor Q2 serves four purposes. It protects against intermittent switching during overload conditions, it turns the SCR off, it discharges the timing capacitor in the relaxation oscillator circuit to assure fairly accurate timing periods, and it prevents timer oscillation during normal operating conditions.

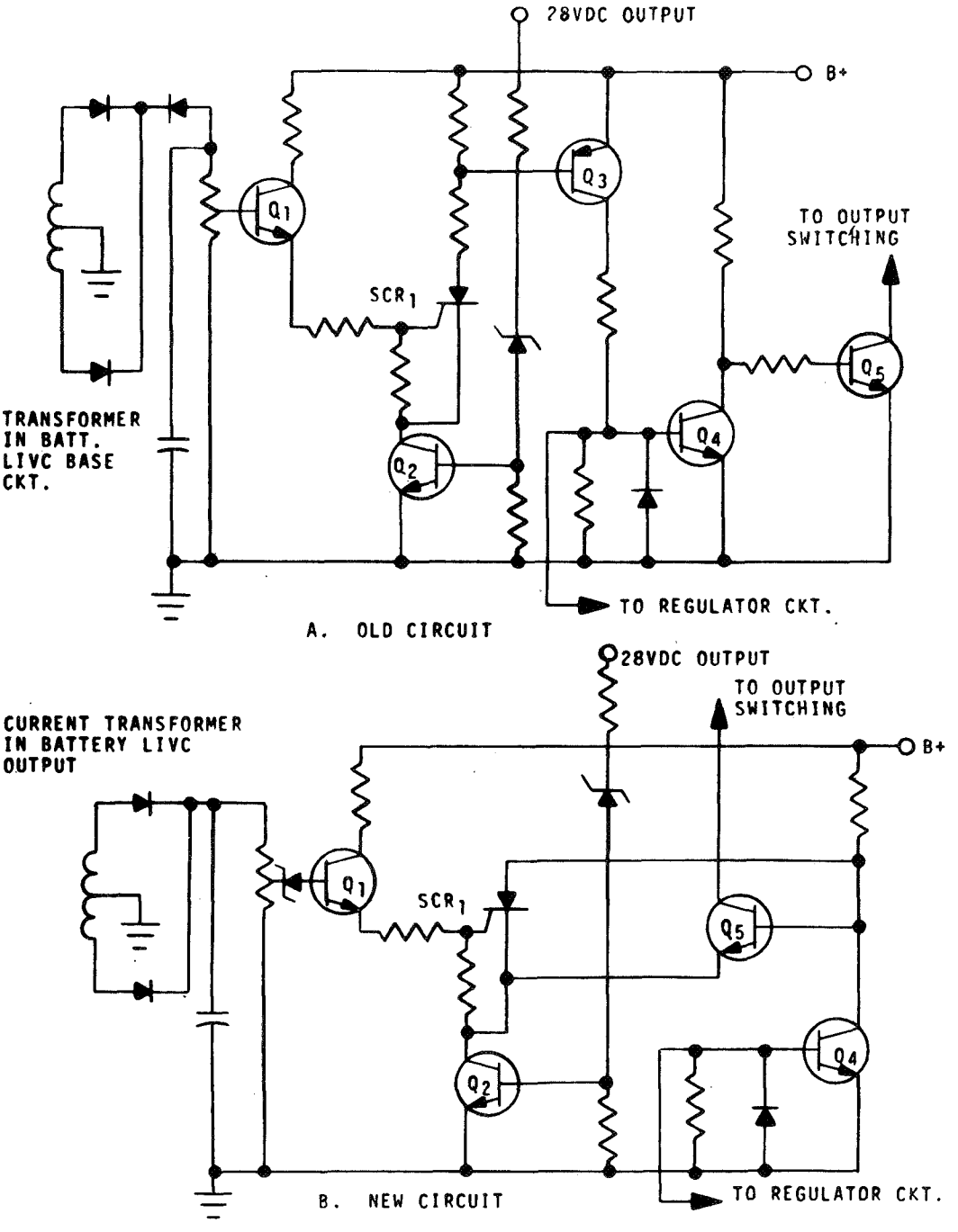


Figure 25. Overload Protection Circuits

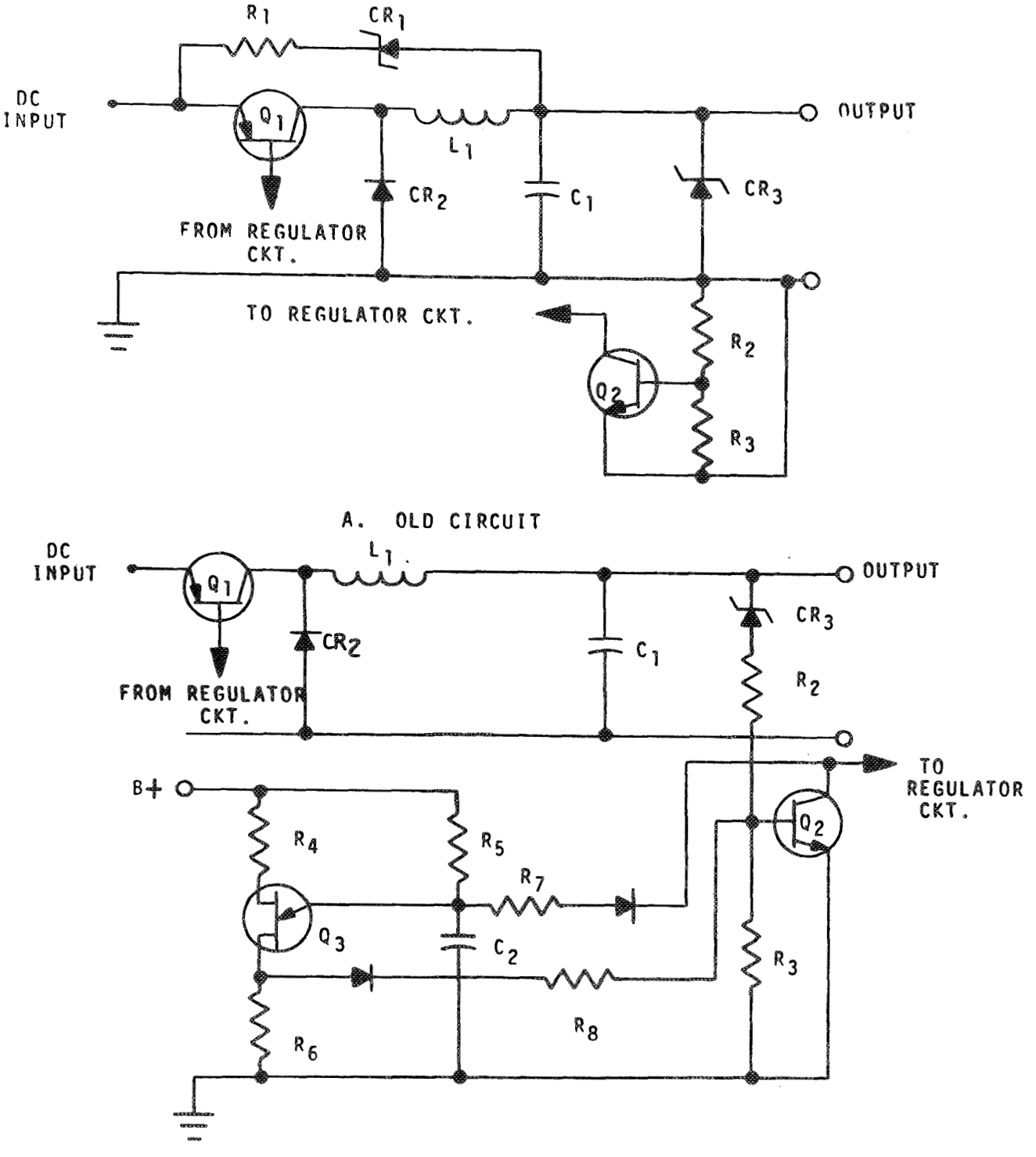


Figure 26. Overload Removal Sensing Circuits

It can be seen that the overload sensing circuit was simplified by removal of several components. The overload removal sensing circuit is more complex; however, the components R1 and CR1 (Figure 26) were physically large, high wattage components that dissipated considerable heat during overload conditions. This required a good heat sink (more volume and weight) for components that may seldom, if ever, be used.

One other modification has been made in the overload protection circuit. Current sensing was originally accomplished from a winding on the battery LIVC base transformer. It was decided that accurate sensing could not be accomplished from this source. The reason for this is because the voltage reflected in the sensing windings is proportional to base-emitter junction voltages of the inverter power transistors. The problems created by this have been discussed in detail previously. Using this source for sensing resulted in considerable variation in the overload cutoff point from one day to the next and sometimes from one run to the next. A current transformer was designed and inserted in the output of the battery LIVC. A winding on this transformer is used to supply the voltage for overload sensing. This transformer measures the battery LIVC load current directly and results in stable operation of the overload sensing circuit.

An attempt was made to use the current drive transformer in the output of the regulator as a source for overload sensing; however, this was unsuccessful. In this case, the voltage developed for one portion of the cycle was again proportional to base-emitter junction voltages. For the other portion of the cycle the load sensing impedance would limit the reset voltage and the reset times would be too long.

This circuit was calibrated to turn off the output regulator at a battery current level of 100 amperes. A degraded cell was simulated with a 135-watt load on the output. When the simulated battery voltage was reduced to 1.35 volts (the degraded cell sensing point), the battery current reached 100 amperes and the overload circuit operated and turned the output regulator

off. It appears that the overload set point will have to be larger than 100 amperes, because the battery current will exceed that value when the battery reaches the degraded point and is being discharged through the discharge transistors (the above test was conducted with the simulated battery connected directly to the input of the battery LIVC). This may create somewhat of a problem because the power transistors being used in the battery discharge circuit and LIVC are rated at 50 amperes. Two of these are used in parallel in both sides of the inverter and in the discharge circuit. The inverter transistors will probably be all right because they operate at 50 percent duty cycle; however, the discharge transistors do not. One salvation may be that when the battery degrades it may degrade rapidly and the excess current may appear for a very short period of time. If this time is long enough to degrade the transistors, it will become necessary to change the power transistor portion of the discharge circuit and use three transistors in parallel. One advantage in doing this is that the overall efficiency will be improved because of lower saturation voltage in the discharge circuit.

g. Battery Charger – The battery charger for this system has some special requirements. It must charge the batteries at a 5-ampere rate up to a 1.98-volt level and not exceed a 2.0-volt level. If the battery charging voltage is allowed to exceed 2 volts for a significant portion of time, the battery will start gassing, build up internal pressures, and explode. At first it appeared that this may require an extremely sensitive sensing and control circuit; however, subsequent testing showed that once the battery is fully charged the terminal voltage rises above 2 volts in a few seconds, and even if the voltage is allowed to rise slightly above the 2-volt level before turnoff time, the time the battery voltage is above that level is not long enough to create a dangerous gassing condition.

In the interest of efficiency it was decided to use a pulse width-modulated type regulator for the battery charger. A magnetic amplifier was considered initially for current sensing; however, this approach was discarded in favor of a new and unique current sensing system designed specifically

for this application. The theory of operation of the initial design of the battery charger is described below. A block diagram of the system is shown in Figure 27 and the schematic in Figure 28.

The regulator transistor, Q1, is controlled through a current amplifier, from a flip-flop which is set by a pulse from a unijunction oscillator and cleared by a pulse from a second unijunction oscillator. The unijunction timers are synchronized to start simultaneously, but the turnoff timer, controlled indirectly by the charge current, times out sooner than the turn-on timer.

A cell voltage threshold detector monitors the cell voltage and when full charge is reached, a disable signal is applied to the turnon timer. This results in complete stoppage of charge current. A reset signal is applied to the cell voltage sensor for the RTG voltage sensor when high current is demanded from the system. The turnon timer is enabled during low power (25 to 45 watts) drain conditions.

The method for sensing the load (charging) current is believed to be unique and an invention disclosure has been turned over to the patent department. The load current sensor operates by sampling the current sustained by inductor L2 through the freewheeling leg of the circuit for a short period of time after Q1 turns off. The current is sampled by turning on transistor Q2, which permits the load current to flow through the pulse transformer, T1, primary winding. The transformer turns N1 and N2 (primary and secondary number of turns) and the resistance R_s are chosen so that the combined volt drop across the pulse transformer, T1, primary, and the turned-on transistor, Q2, is less than the forward volt drop across the silicon diode, CR1. As a result, an insignificant portion of the load current flows through diode CR1 during the sample time. When transistor Q2 is turned off, the load current flows through diode CR1 until transistor Q1 turns on again. (See Figure 29, Timing Chain Diagram.) While the load current flows through N1 of T1, a voltage is developed across R_s of the value $V_{Rs} = (\frac{N1}{N2} Rs)\, I_{LOAD}$.

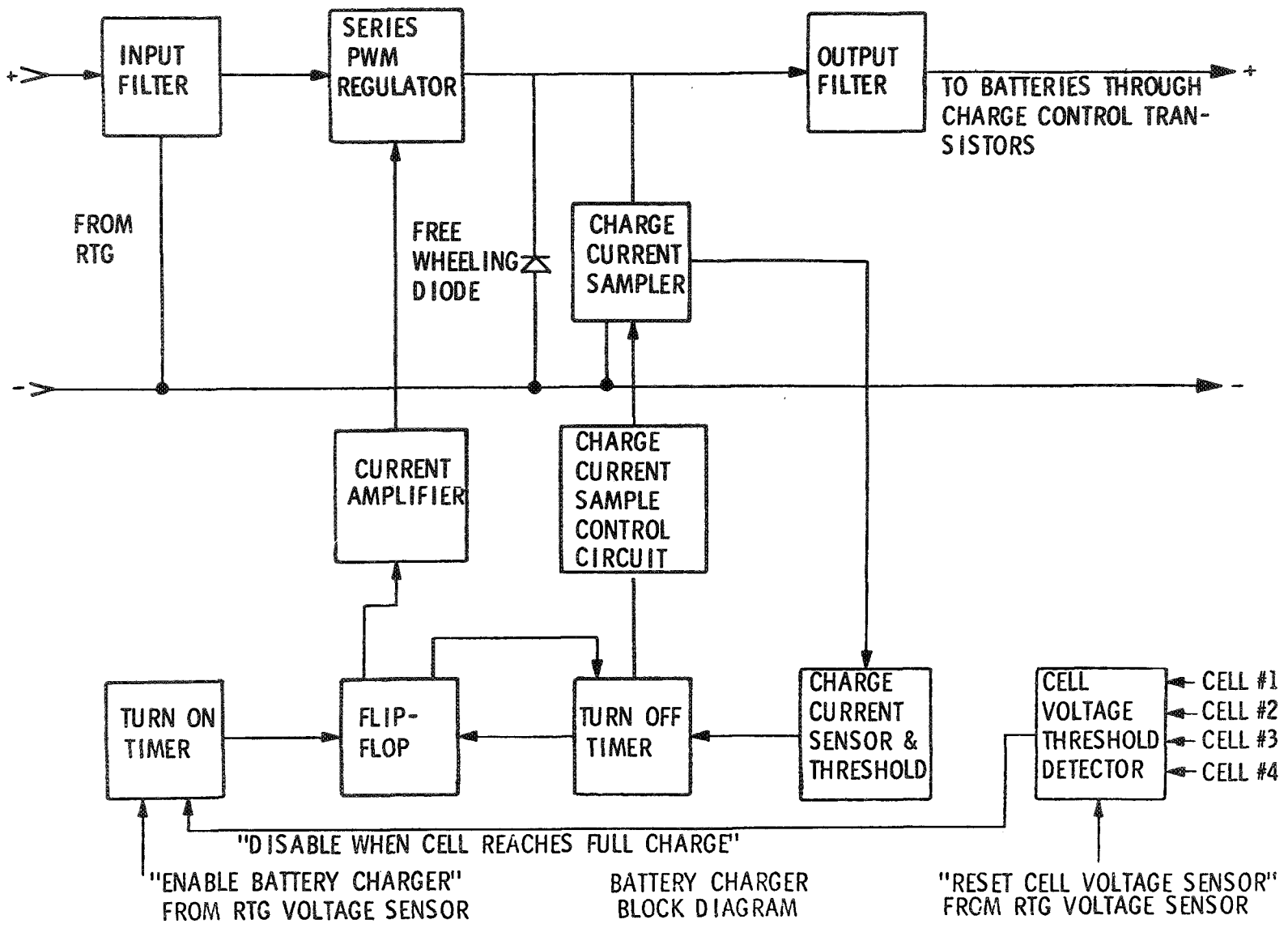


Figure 27. Battery Charger Block Diagram

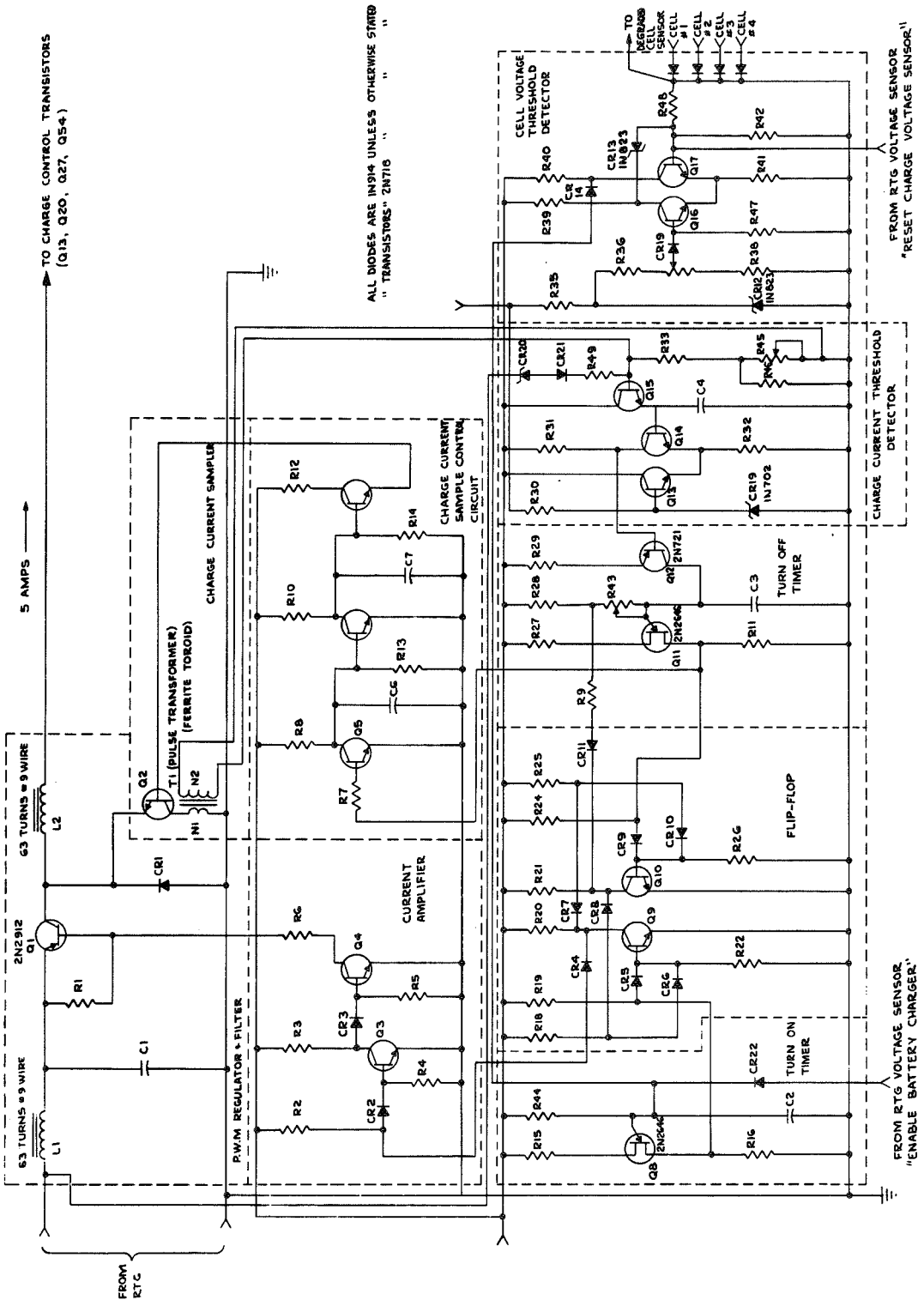


Figure 28. Battery Charger Circuit

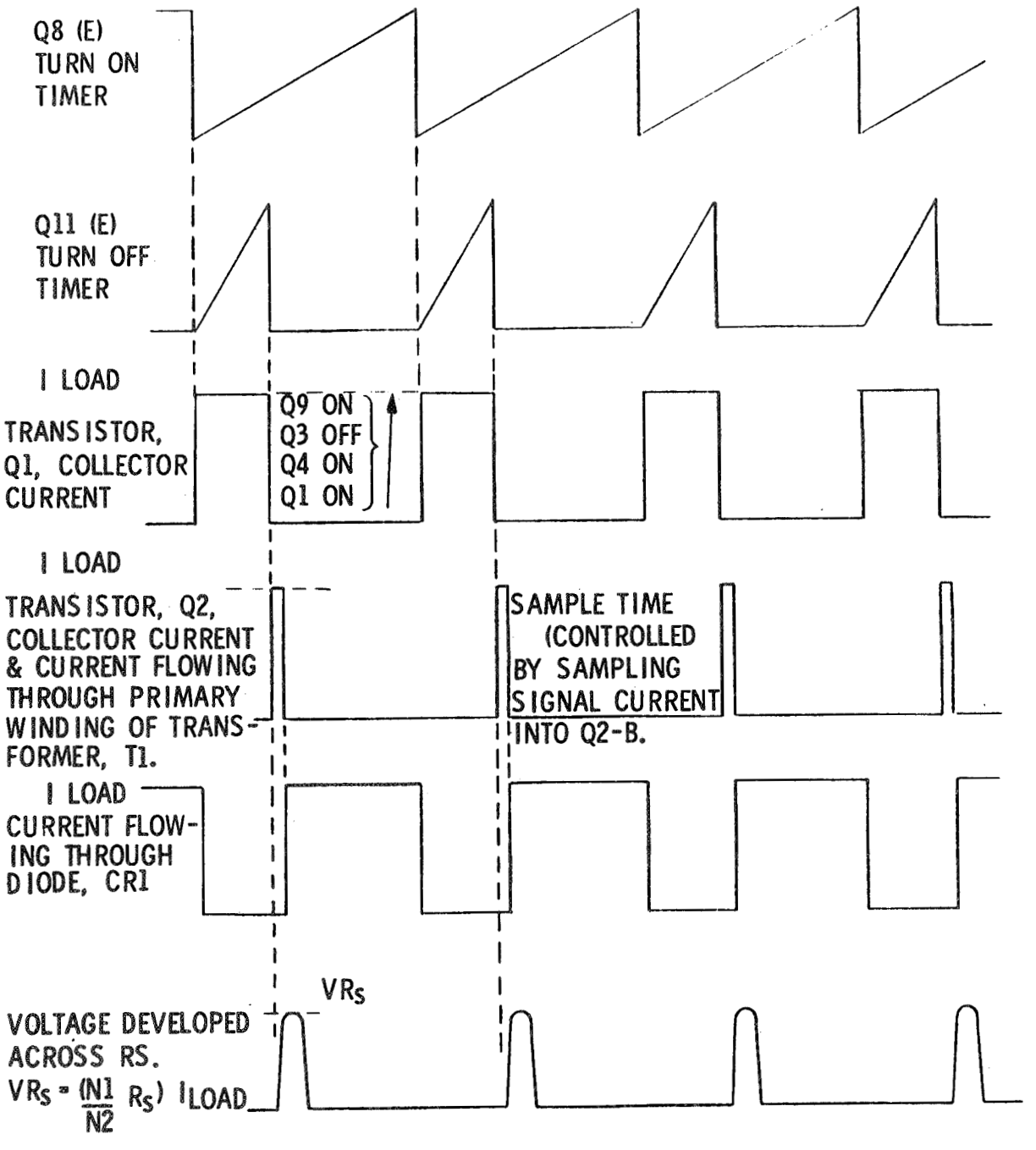


Figure 29. Battery Charger - Timing Chain Diagram

Some advantages of this current-sensing circuit over most conventional methods are:

1) It consumes no additional power from the load circuit.

2) No series dropping device is required between the load and common ground.

3) The sensor can be very small, even for very large currents, since it only operates for short portions of the duty cycle.

4) The voltage across R_s, which is proportional to the load current, can easily be made to match the voltage levels of the threshold detecting circuitry.

5) No. D. C. amplifier is required to get the sensed current to a convenient voltage signal level.

Another change was a modification in the regular portion of the battery charger. The transistor Q43, Figure 30, was originally connected in the emitter follower configuration. This type configuration creates a problem because it presents a variable impedance to the drive circuit if the collector current varies. In this case the collector current is the sawtooth current of the unijunction oscillator. This sawtooth waveform is reflected back to the drive circuit and creates some instability when the regulator is operating at the maximum "on time" or maximum "off time" points. The circuit was changed to the common emitter configuration to eliminate the unstable conditions. Some of the resistance and capacitance values in the unijunction oscillator circuits were changed to increase the operating frequency of the regulator. This resulted in better current regulation.

Another problem encountered was that when a degraded cell was sensed during the discharge mode, the regulator would go out of control momentarily when the system switched to a charge mode after the peak load was removed. This was caused by the new battery being simulated by a short

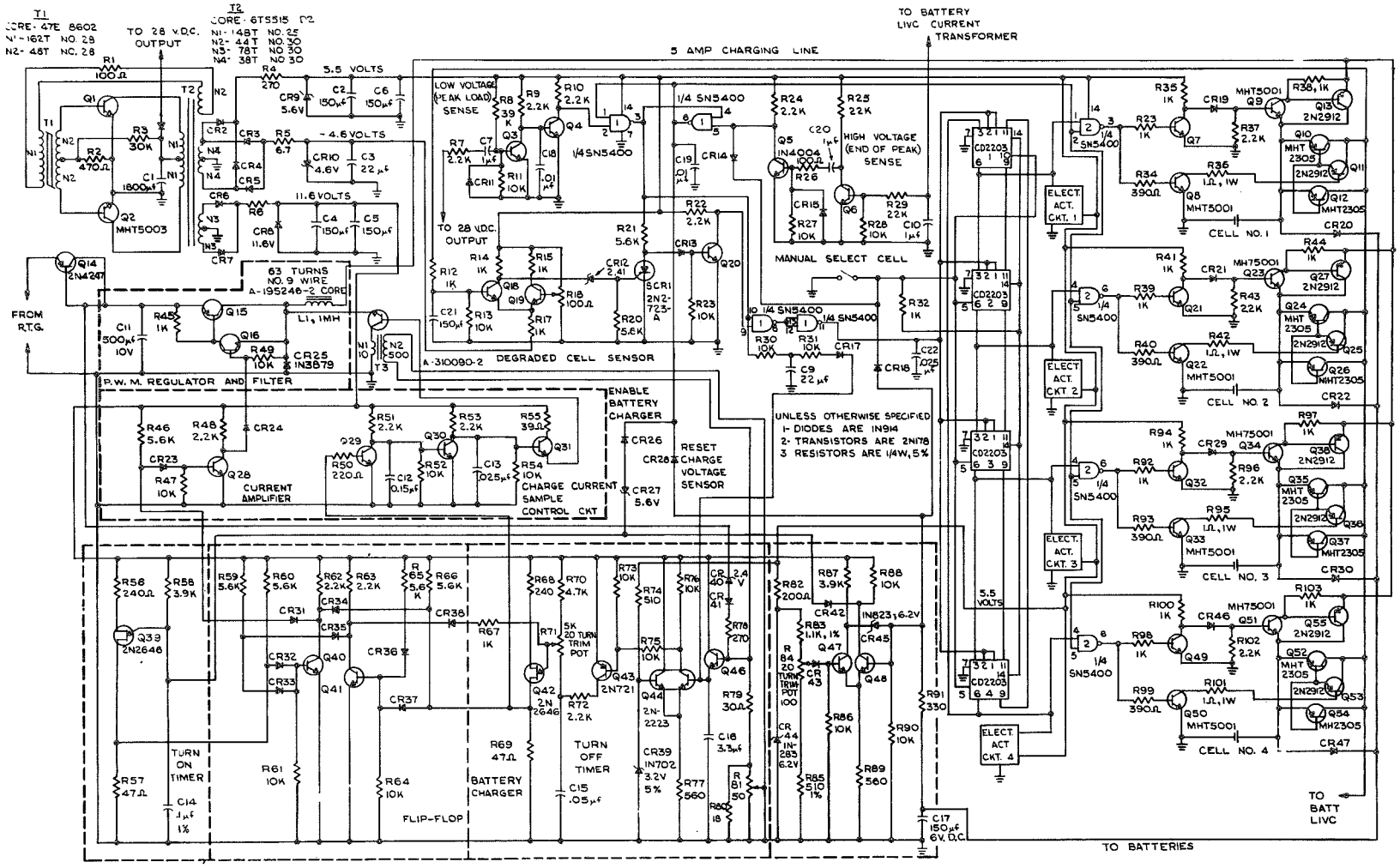


Figure 30. Battery Charging and Sequencing Circuits

circuit and the current sensing circuit not reacting enough to limit the initial charging current. This current surge would pull the simulated RTG voltage down very low, resulting in a loss in regulation of the 28-volt output, and the system would go out of control. The output regulator turned off completely and the system waited three seconds before the output regulator turned on again. This would reset the logic system back to the initial conditions. This problem was solved by connecting a biasing network from pin 3 of number one nand gate (see Figure 30) to capacitor C in the emitter of Q46 in the current-sensing circuit. This bias network provides a voltage on C16 when the system is in the discharge mode. When the system switches to the charge mode, the charge on capacitor C16 is higher than normal. This creates a maximum off, or lower charging current, condition in the regulator. The charge on capacitor C16 will decrease and the charge current will increase to 5 amperes. A delay was incorporated into the bias system to slow the transition from the low charge rate to the normal charge rate.

The clamping network consisting of resistor R67 and diode CR38 is now returned to the charging capacitor C15 instead of the top side of the calibrating potentiometer R71. This was done to improve the clamping action. The value of resistor R67 was lowered for the same reason.

An effort to improve the efficiency of the battery charger was made by using an augmented or Darlington circuit in the line switch. This improved the efficiency at medium and high input voltage levels but showed no improvement at the low input voltage levels. Another problem with this circuit is that if the drive transistor switches on very much faster than the power transistor it will try to supply all of the load current and burn out. For this reason this approach was discarded.

The next modifications made in the battery charger circuit can be seen in the schematic, Figure 30. The power input to the battery charger has been modified. A diode-connected transistor is used to isolate the power input

from the RTG LIVC, and the input filter choke was removed. The diode is necessary to isolate the input filter capacitor from the LIVC and prevent high-current surges in the LIVC power transistors when the overvoltage circuit operates. The input capacitor could be removed and a choke input type filter used. The choke acts as a buffer and may eliminate the need for a diode; however, when the overvoltage circuit operates with this choke in the system, the charging system will oscillate at a low frequency rate and the battery charging rate varies. The best combination appears to be to use a diode to isolate the input and not using the choke. This also saves on weight and volume. The value of the input capacitor was lowered. For some reason, a certain amount of instability occurs if the value of this capacitor is too large.

A new method of current-sensing was developed for the battery charger. This method uses a transformer in the charging line similar to the one used in the output line of the 28-volt output regulator. The transformer is connected into the system in the same manner. The secondary output of the transformer is half wave rectified. The voltage developed in the secondary from the forward charge current in the primary is filtered and fed to the input of regulator. There is no output load on the secondary for the voltage developed from the freewheeling current. This results in a very rapid and reset action of the core of the sensing transformer. This method of current sensing seems to be just as effective and is much more simple than the original method. This method uses four less transistors and associated components.

Further testing of the battery charger resulted in several more modifications in the circuit. One of the modifications was in the clamping circuit of the turnoff unijunction oscillator circuit. This oscillator was originally clamped off when the turnon unijunction oscillator capacitor was charging. The clamping action was accomplished by using a resistor-diode combination connected from the charging network in the turnoff oscillator to the collector of Q41 (Figure 31). If the resistor value is too small the flip-flop will

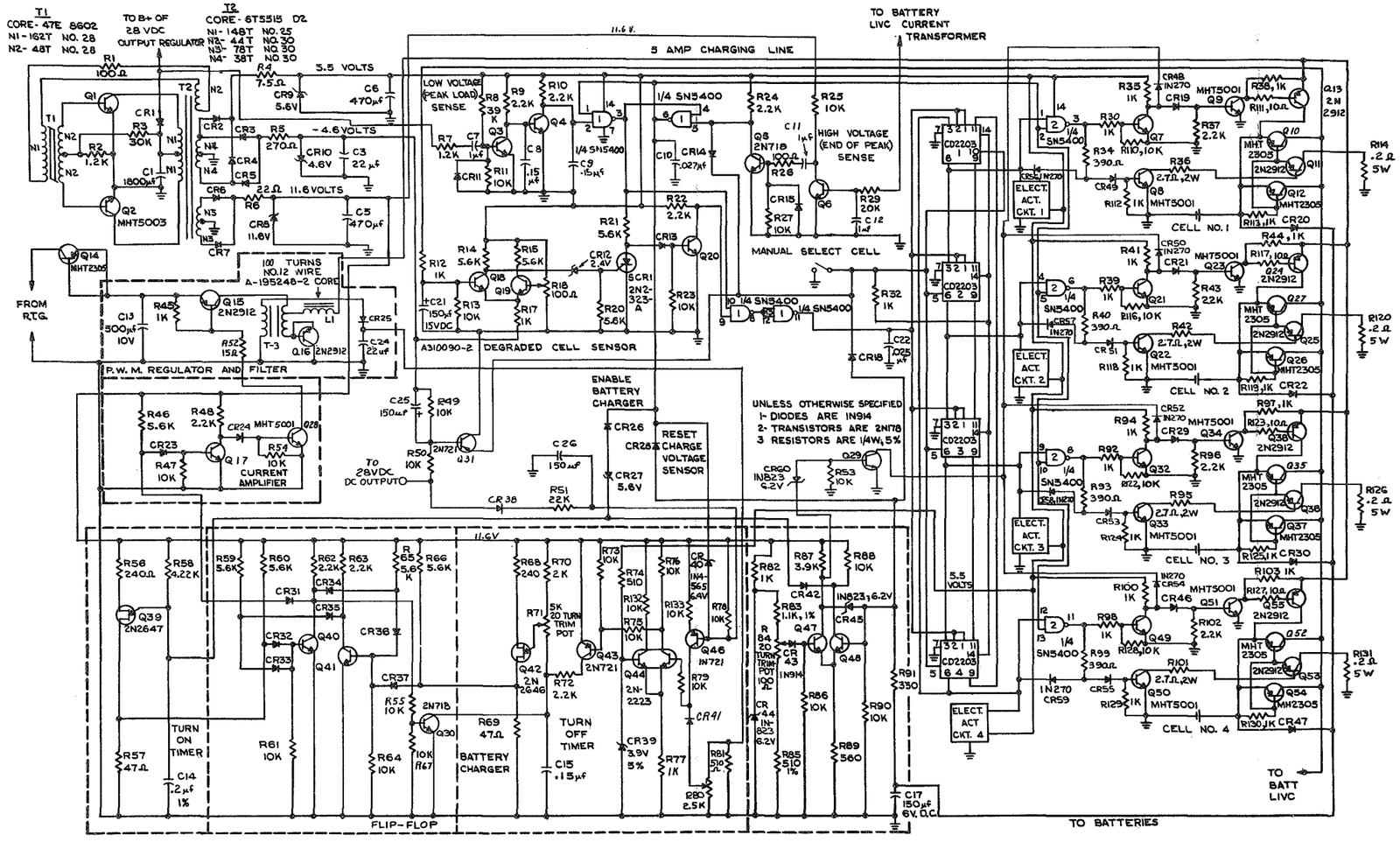


Figure 31. Final Configuration of Battery Charging and Sequencing Circuits

not work. This approach does not provide good clamping action. This is because the resistor in the clamping network is part of a voltage-dividing network consisting of this resistor and the potentiometer and resistor in the oscillator RC network. The capacitor in the oscillator will charge up to the voltage that can appear across the clamping resistor during clamping action. This means that the voltage on the capacitor at the start of the off time will vary with the length of the on time. This affects the accuracy of control of the 5-ampere charge rate and it limits the control range. This problem was eliminated by using a transistor (Q30, Figure 31) to do the clamping action. Use of this type clamping circuit improved regulation and stability of the charger.

A different type delay circuit was designed for delay of charge after initial turnon and after the peak load cycle. Redesign of this circuit was necessary because the original delay circuit was not compatible with the new current sensing circuit. The delay is accomplished by turning on Q46 (Figure 31) and applying a voltage to the input of the charger differential amplifier. This simulates a high charging current and maintains a zero charging current. Transistor Q46 will stay on until capacitor C26 charges. The delay time can be changed by changing the value of C26.

It was necessary to add a turnoff circuit to the output switch in the charger line. This transistor (Q13 in line 1) was originally left on at the end of the charging cycle. Charging turnoff was accomplished by turning off the pulse width-modulating transistor Q15. If the output transistor is not turned off, a discharge path for the battery occurs through the collector to base junction (see Q13), through a 10-ohm resistor, and through the drive transistor (see Q9). The turnoff circuit transistor Q29 is turned and turns off the output drive transistor. Transistor Q9 obtains its turnon signal from the maximum charge voltage sensing circuit.

h. Battery Sequencing Circuitry – The battery sequencing circuit consists of the subassemblies listed below:

1. RTG-Voltage Sensing – This circuit senses when the peak load is applied to the system. When a peak load is sensed, the circuit disables the charge control and enables battery discharge control.

2. High-Voltage Sensing Circuit – This circuit senses when the battery cell is fully charged and then disables the charging operation.

3. Low-Voltage Sensing – This circuit senses when a loaded battery cell is degraded and, subsequently, causes the degraded cell to be switched out and a new cell selected and activated.

4. Sequencing Circuit – Upon initiation of the power supply, this circuit selects silver-zinc battery cell No. 1 and connects it into the circuit by sold-state switching. Thereafter, cell No. 1 will remain connected until the low-voltage sensing circuit applies a signal to the sequencing circuit to activate and select a new cell and connect it into the circuit, while the previously used cell is removed by solid-state switching. This circuit sequentially selects a new battery cell, (1, 2, 3 and 4) and sequentially removes the degraded cell as indicated.

5. Activation Circuits – This circuitry controls electrolyte activation of the newly selected battery. Design of this circuitry has not been completed because additional information is required on activation requirements for the particular silver-zinc battery specified for use.

6. Charge and Discharge Control – This circuit controls the charge and discharge current of the selected battery cell. The first design of the logic and sequencing circuits is illustrated in Figures 32, 33, and 34. A discussion of the subassemblies of this design effort follows:

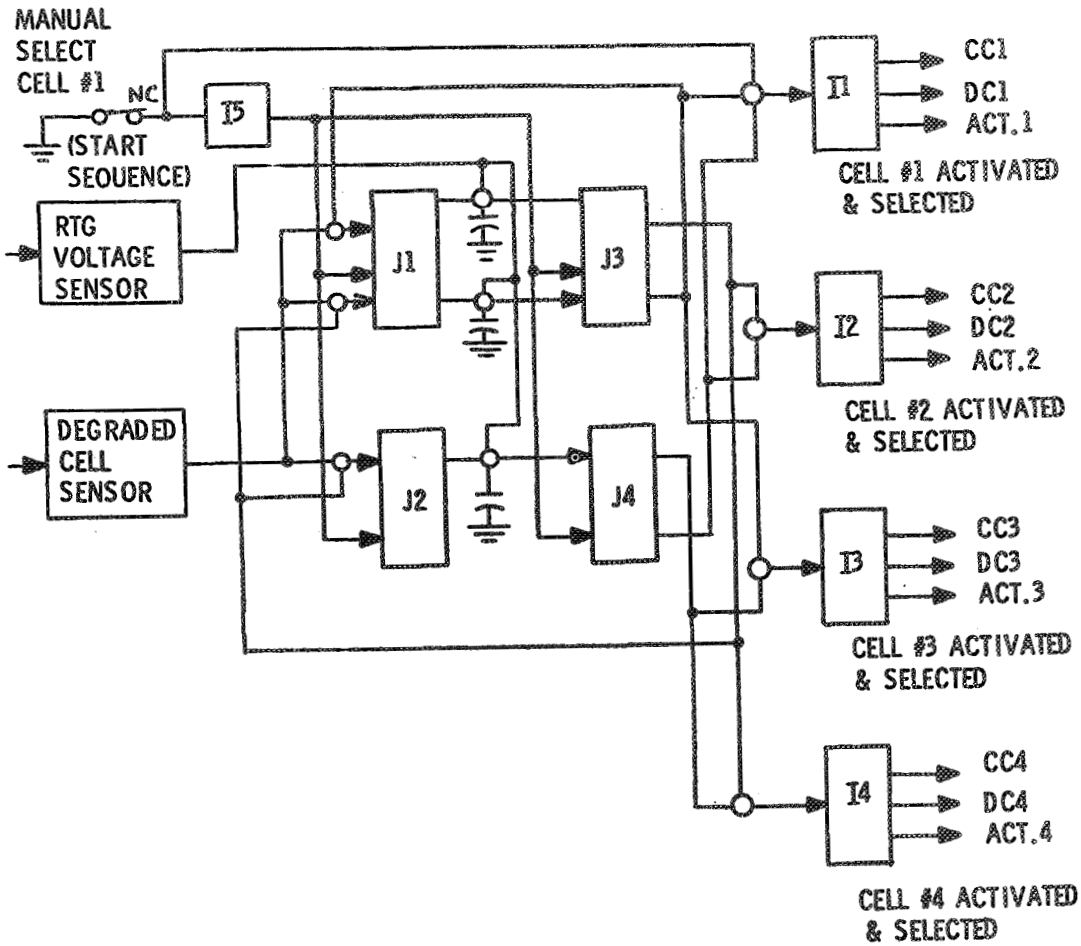


Figure 32. Battery Cell Sequencing, Block Diagram.

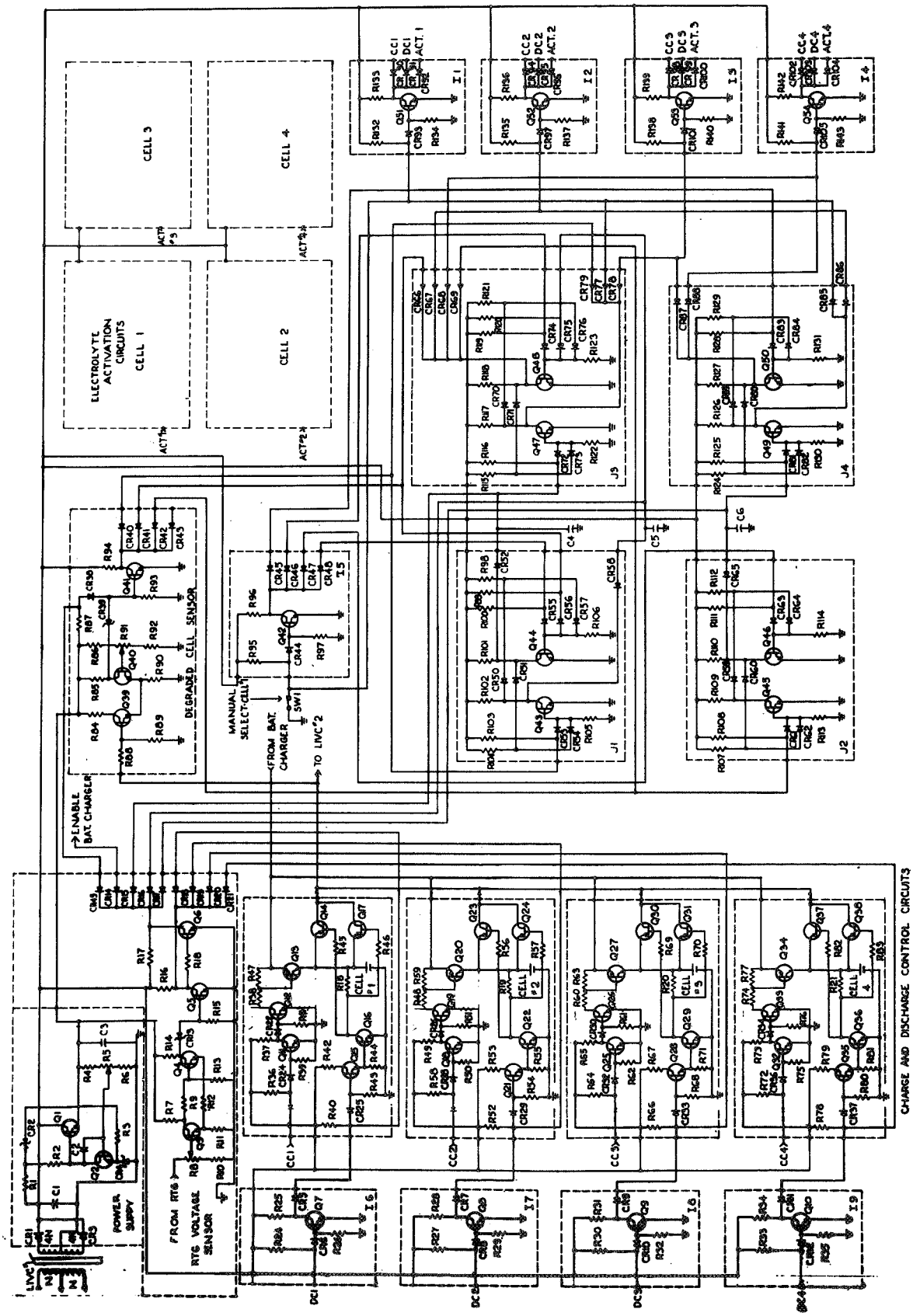


Figure 33. Battery Cell Sequencing Circuit

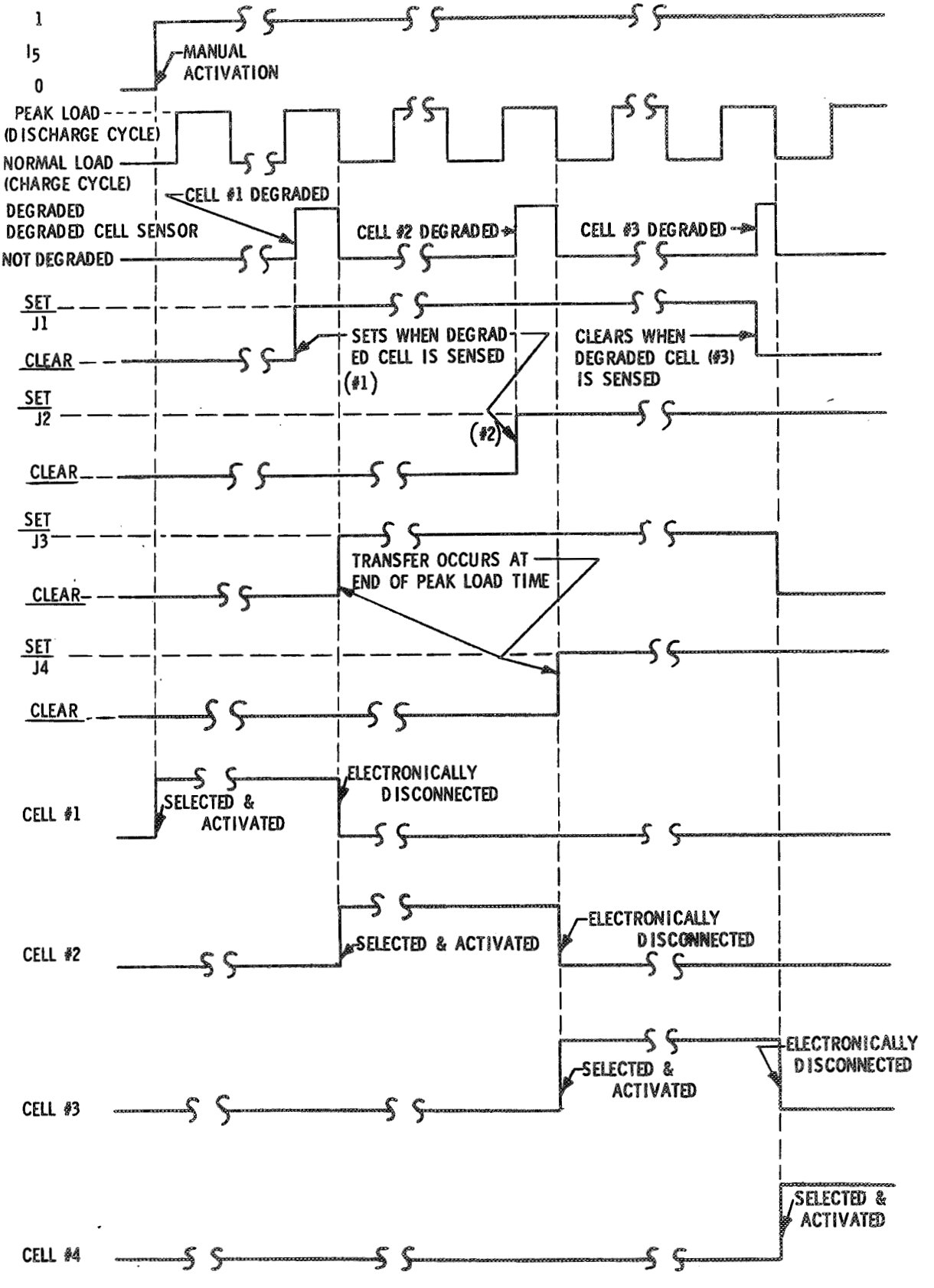


Figure 34. Battery Cell Sequencing Time Chain

1. RTG-Voltage Sensing (Figure 33) – This circuit, which senses when the peak load is applied to the system, consists of a Schmitt trigger which switches when the RTG voltage drops several tenths of a volt below its "nonpeak load" level, due to increased loading. The Schmitt trigger output is converted to a logic level signal which disables the charge control circuits, enables the discharge control, and inhibits selection of a new cell (when a cell becomes degraded) during peak load time.

2. High-Voltage Sensing Circuit – This circuit, which senses when the battery cell is fully charged, has been incorporated in the battery charger circuit.

3. Low-Voltage Sensing Circuit – This circuit, which senses when a loaded battery cell is degraded, consists of a differential detector and a logic circuit which advances a flip-flop counter when a battery cell is degraded. The voltage is sensed on the collectors of the discharge control transistors which are common for all four cells.

4. Sequencing Circuit – This circuit controls selection and activation of each battery cell in sequence. The first cell is selected by a manual command and each succeeding cell is selected upon sensing. When the cell in use becomes degraded (during the peak load time), a flip-flop counter is advanced (see Figure 34). At the end of the peak load time, information in the counter is transferred to another set of flip-flops enabling the next battery activation circuit, and the charge and discharge controls of the next battery.

The first modification made in this design was made in the battery discharge switching circuit and is shown in Figure 35A. The original circuit is shown in Figure 35B. When the complete system was first hooked up and a heavy load was put on the output, the battery discharge transistor would not turn on completely. The system would "hang up" in this condition because the

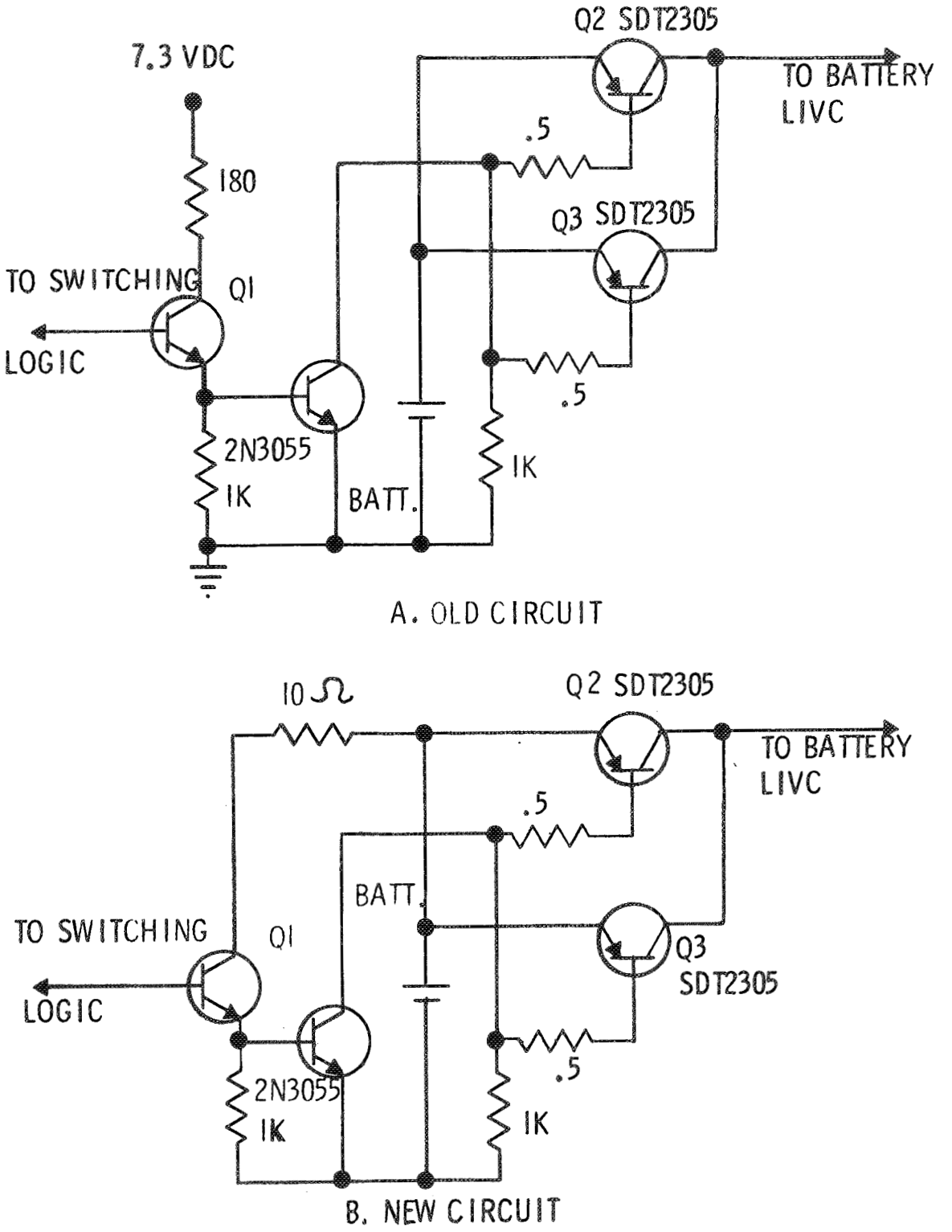


Figure 35. Battery Discharge Switching Circuit

battery LIVC would not take over the load, the RTG output voltage would stay at a low value, the normal 7.3-VDC supply would be at a much lower value, and sufficient drive for the discharge circuit would never be attained. This problem was eliminated by obtaining the initial drive current from the battery, as shown in Figure 35B. The configuration shown in Figure 35B is also more efficient because the loss across the 10 ohms connected to the battery is less than the power loss across the 180 ohms connected to the 7.3-VDC.

The 12-VDC supply and 7.3-VDC supply for the logic and sequencing circuits were originally obtained through a series-type regulator. This, of course, is a very inefficient type of regulator. When this supply and the associated circuits were connected to the system when there was a nominal load on the output, the RTG current would increase about 7 amperes (from 8 to 15 amperes) with no battery charging. It was obvious that a low-loss, regulated-type supply was necessary. A separate pulse width-modulated regulated power supply was considered; however, this would add another complex subsystem to the overall system. It was decided to use the 28-VDC output as a supply for an inverter with 12- and 6-volt outputs from the inverter. The supply would not need to be regulated because the source was very well regulated and load variations in the system were not great enough to produce significant output variations due to voltage drops across the inverter impedance. An inverter was designed for this purpose. This inverter was not a self-oscillating type inverter (see Figure 33). The base drive for the inverter transistors is obtained from an output winding on the RTG LIVC. With this supply connected under the same conditions as stated previously, the RTG current increased about 1.5 amperes.

Another problem encountered in this system was loss of memory when a large load was put on the output. The 90-watt LIVC would turn on and supply energy for the extra load, but when the load was removed the charger would try to charge the next battery. The system acted as if it had sensed a degraded battery. Investigation showed that this was caused by a loss of

memory in the system when the RTG voltage was pulled down to a very low value when the peak load was connected to the output. There is a short period of time (the time required for the battery LIVC to activate) when all voltages in the system are very low. This problem was corrected somewhat by isolating the logic and sequencing circuits power supply from the 28-VDC output with a diode, connecting a 150-uf capacitor to ground at that point, and connecting 150-uf capacitors across the 12- and 6-VCD outputs. The problem still exists when the battery LIVC is slow in turning on.

The next design change was a major one. Much of the sequencing circuit was changed from discrete components to integrated circuits. The redesigned system is shown in Figure 31. Logic diagrams of the integrated circuit portions of the system are shown in Figures 36 through 40. Positive 1 logic language is used in these figures. The integrated circuit portion of the logic consists of two quad-dual input nand gates and four J-K flip-flops. Truth tables for the integrated circuits, as connected in the system, are shown in Table 1.

Figure 36 shows the condition of the outputs of the integrated circuits for the initial conditions and charge mode. Actual charge or no charge is determined by the battery charger input logic. It can be seen in Figure 36 that all of the outputs of all the unused discharge circuits are in the 1 or on mode. This can be done because the batteries cannot discharge until they are initiated. The reason for having this condition is to provide a method of discharging a degraded battery after it has been switched from the system. The degraded battery voltage will probably not be high enough to contribute to the load when the peak load is on and the new battery is providing the power for the peak load; however, the degraded battery will discharge completely through the discharge transistor's drive circuit (see Figure 31). Once the battery has been degraded and the system has switched to a new battery, the degraded battery will always be clamped to ground through the drive circuit.

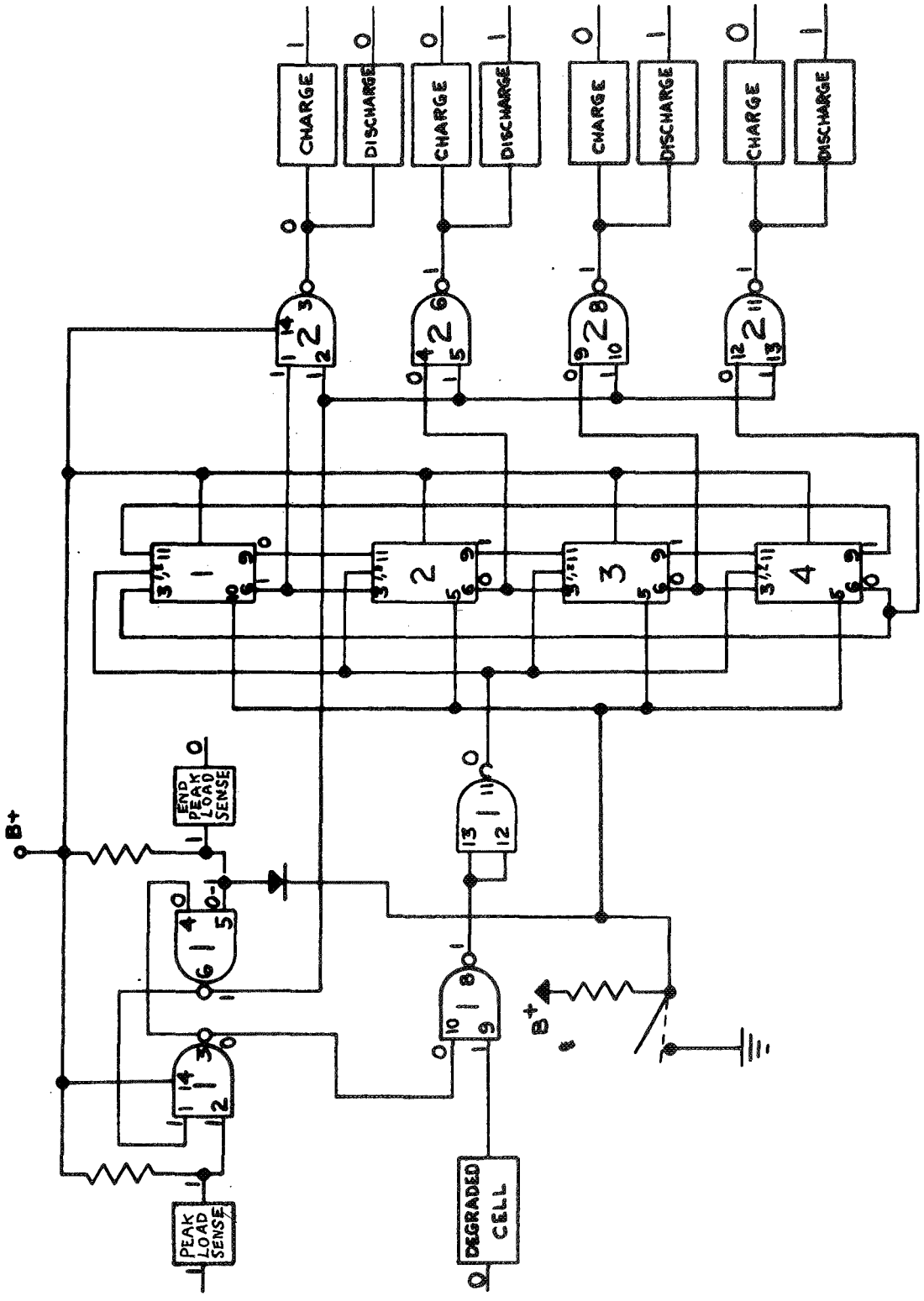


Figure 36. Initial Steady State Charge Mode

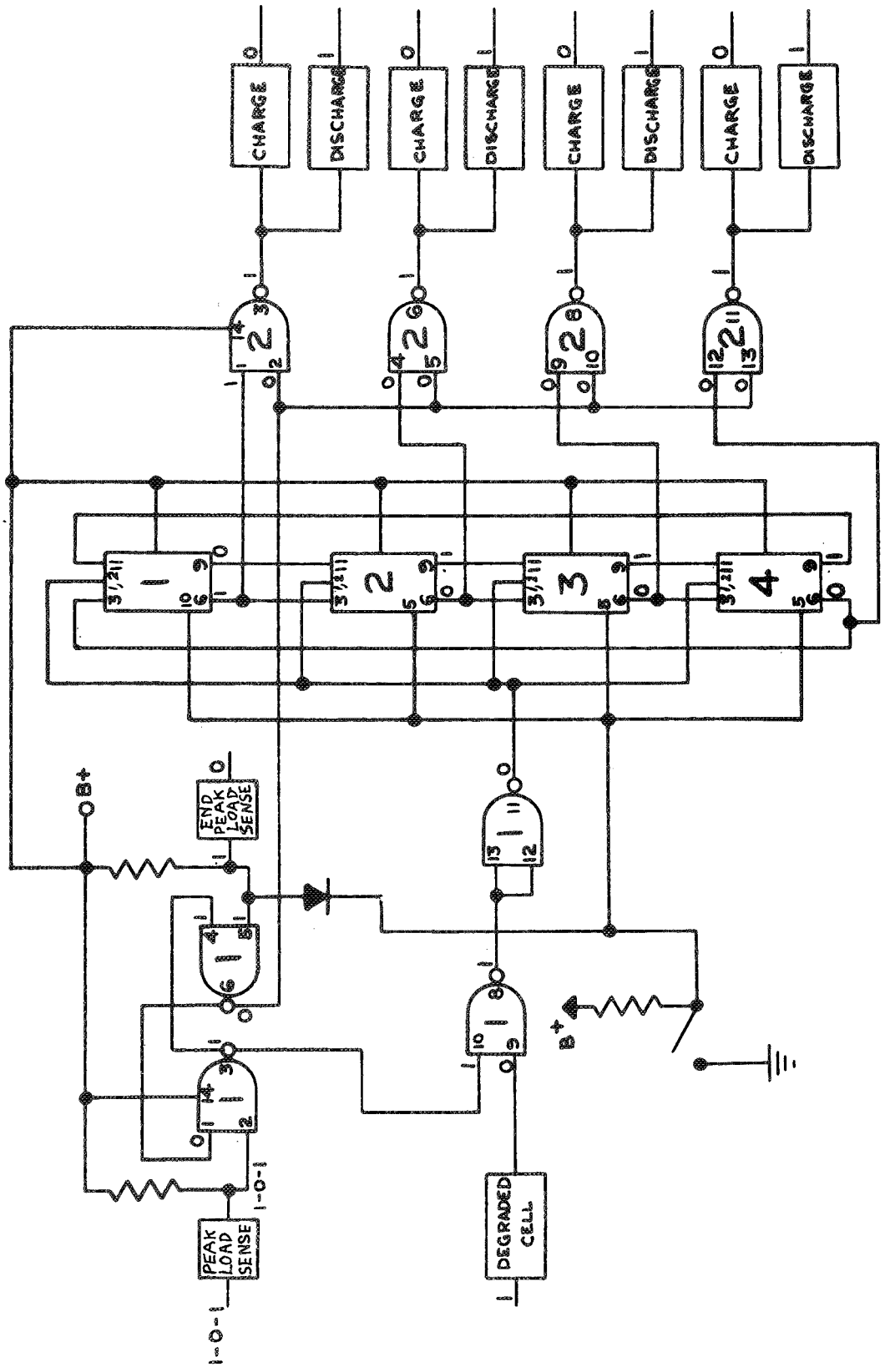


Figure 37. Turnon and Steady State Discharge Mode

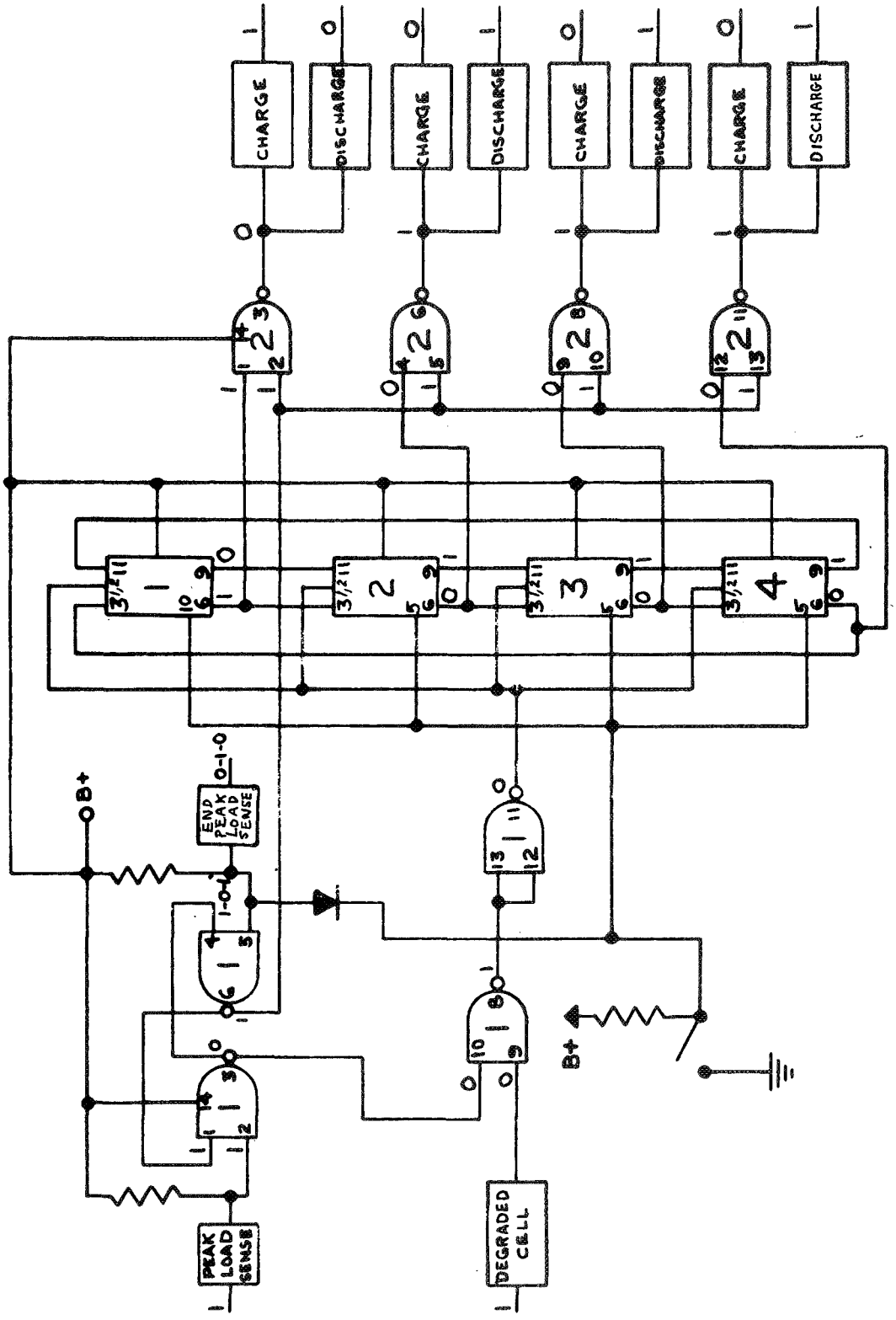


Figure 38. Discharge to Steady State Charge Mode

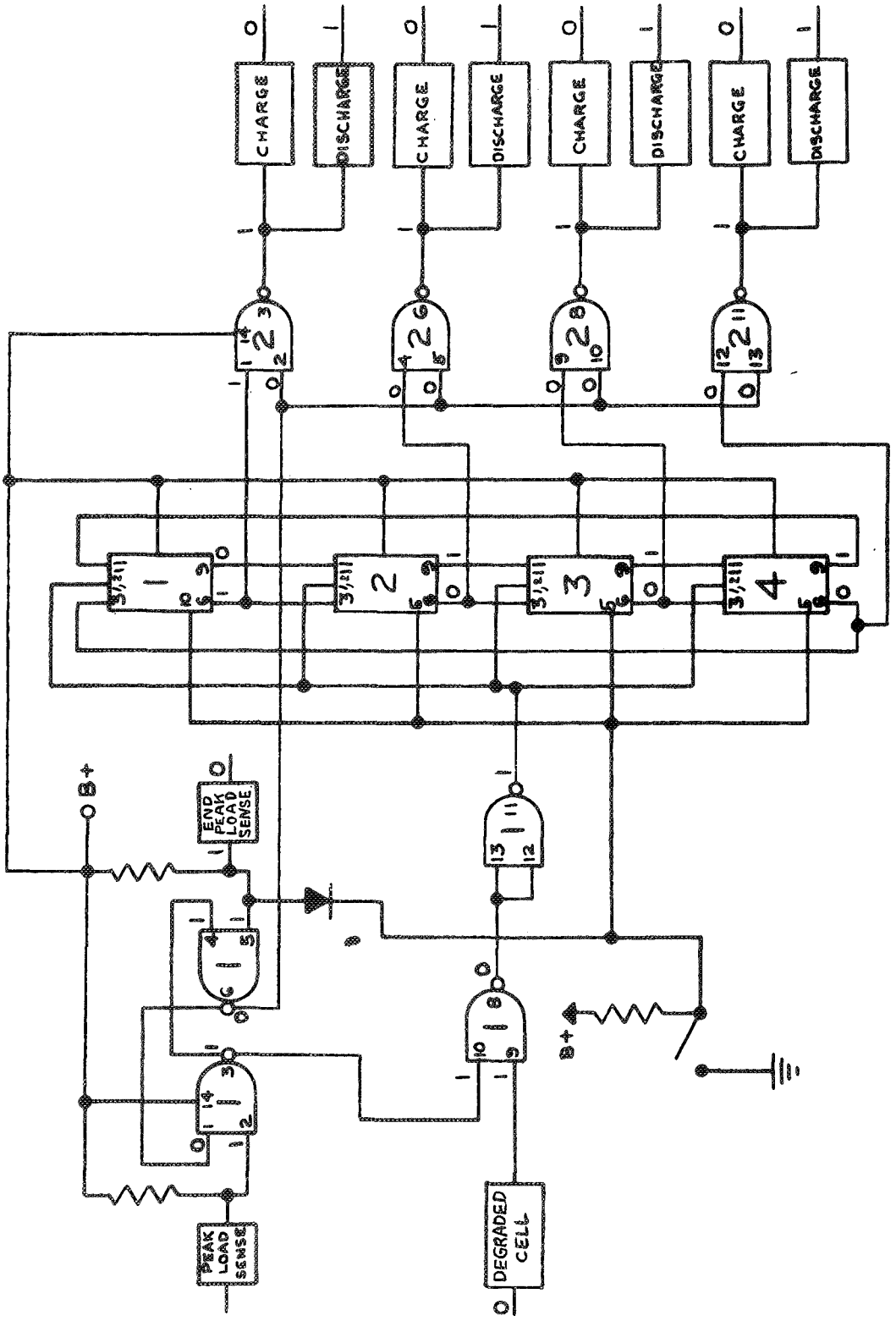


Figure 39. Steady State Discharge Mode with Degraded Cell Sensing

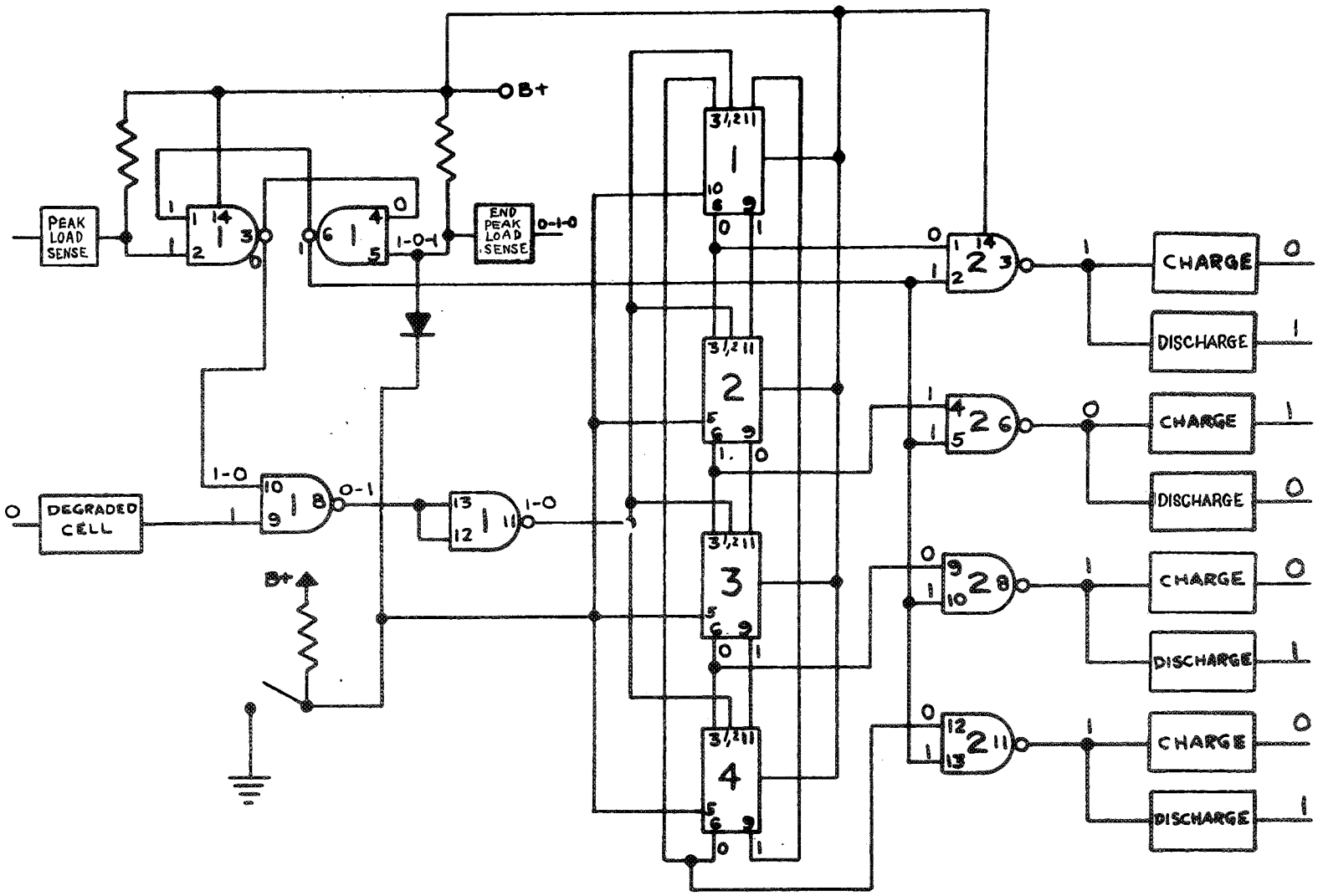


Figure 40. Discharge to Steady State Charge after Degradation Cell Sensing

TABLE 1. Truth Tables

QUAD-DUAL INPUT NAND GATES

INPUTS (1-2, 4-5, 9-10, 12-13)	OUTPUTS (3, 6, 8, 11)
0 0	1
1 0	1
0 1	1
1 1	0

(Outputs are 0 only if both inputs are 1)

J-K FLIP-FLOPS

SET-RESET

INPUTS		OUTPUTS	
10	5	6	9
0	1	1	0
1	0	0	1

CLOCK PULSE

INPUTS		OUTPUTS			
3	11	6		9	
		From	To	From	To
0	1	1	0	0	1
1	0	0	1	1	0

Figure 37 shows the condition of the outputs for discharge turnon and steady state discharge mode. The input for switching to this mode is a differential pulse that goes from 1 to 0 to 1. This signal is obtained from the 28-volt D. C. output (see Figure 31). When peak load is applied, this output drops momentarily until the battery LIVC turns on. This voltage change is capacity-coupled to the input of the peak load-sensing circuit. It can be seen that all of the circuits are in a discharge mode; however, as explained previously, this should create no problem.

Figure 38 shows the condition of the outputs when the end of peak load is sensed and the system returns to the battery charging mode. The input for switching to this mode is a differentiated pulse that goes from 0 to 1 to 0. This signal is obtained from transistor Q6, Figure 31. The signal for operating this transistor is obtained from the overload current sensing transformer. When peak load is removed, the battery LIVC will turn off because of insufficient drive. When the battery LIVC turns off, current in the overload current transformer drops to zero and provides the signal for switching to the charge mode.

Figure 39 shows the logic outputs for the discharge mode and degraded battery sensing. The output of pin 11 of the nand gate number 1 rises to 1 at this point. This is the beginning of the clock pulse for switching to the next battery. The first flip-flop will not switch at this point because switching occurs only on the trailing edge of the clock pulse. The trailing edge appears (pin 11 goes from 1 to 0) when the system switches back to the charge mode. This is shown in Figure 40. At this time flip-flop numbers 1 and 2 switch. Battery number one can no longer go into a charge mode. When flip-flop number 2 is switched, battery number two is activated and starts charging. A problem may occur at this point. It will probably be necessary to delay start of charging for a small period of time to allow the electrolyte to enter the battery. The battery will probably look like a high impedance until the electrolyte is distributed. This high impedance would cause the charger to turn on fully to try to drive 5 amperes into the battery.

This full turnon would present over 2 volts to the fully charged battery-sensing circuit, and the charger would turn off. The charging circuit is not reset until the battery goes into a discharge mode. The system would then sense a degraded battery (the new battery that was not charged) and would switch to the next battery after the peak load cycle had passed. This would continue indefinitely and the system would be useless. A delay circuit will be designed and incorporated into the system.

Transients created by operation of the overvoltage circuit caused considerable intermittent switching in the logic switching circuitry. Most of these problems were caused by transients on the peak load-sensing and end of peak load-sensing input circuits. These inputs were connected directly to the RTG. This problem source was eliminated by sensing peak load and end of peak load from other points. This has been explained in detail in an earlier portion of this section. Other problems of intermittent switching were eliminated with use of filter and bypass capacitors in strategic portions of the circuit. These capacitors are C10, C19, and C22 in the schematic, Figure 31.

The degraded cell-sensing circuit was another source of problems with transients. This circuit is essentially a Schmitt Trigger circuit. The type of circuit used in the original design was not a good "snap action" circuit. If a simulated voltage decrease was made on the input to this circuit, the circuit would go into an unstable condition at the switchover point. The unstable condition was due partly to an oscillating condition and partly to amplification of transients at the switchover point. This problem was eliminated by modifying the circuit. This circuit is shown in the schematic, Figure 31. An SCR was inserted in the circuit to obtain "snap action" switching. The voltage for the SCR is supplied from pin number 3 of the number one nand gate. Pin number 3 goes to 0 when the system returns to the nominal load condition. This performs the function of commutating the SCR to an off condition after the discharge or peak load cycle.

The battery discharge switching circuit has been modified. This circuit is shown in the schematic, Figure 31. The power switching circuit has been changed to a Darlington configuration. This circuit has not been tested; however, it is hoped that it will improve the efficiency of the discharge circuit.

A self-oscillating inverter was designed for the logic power supply, shown in the schematic, Figure 31. The power for this inverter is obtained from the 28-volt D. C. output. One problem encountered with this supply is that the 28-volt output drops momentarily when the peak load is applied. This results in a transient in the 11.5 D. C. and 5.5 D. C. supplies. This transient has been minimized by using a 1, 800-uf capacitor (Capacitor C in the schematic) at the input to the inverter and filtering and zenering the outputs. A minus 4.6-volt supply was added to the power supply to provide a negative voltage to the modified degraded cell sensing circuit. The 1, 800-uf capacitor adds another rather bulky component to the system; however, it is necessary to prevent undue transients in the 11.5-, 5.5-, and 4.6-volt supplies. Using the regulated 28-volt output to supply the inverter still appears to be the most practical way of developing the logic voltages efficiently. The zeners in the outputs are biased at very low current values and therefore absorb very little power. The main purpose for them is to prevent circuit burnout due to positive going transients.

An alternate approach is to accomplish the battery sequencing with squib switches (see Figures 41 and 42). Since squib switches will probably be required to activate the cells as they are selected, the entire sequencing logic could be achieved by adding extra contacts and higher current contacts. Redundancy and high reliability would easily be accomplished and power losses minimized.

In the circuit shown in Figures 41 and 42, the battery LIVC (LIVC No. 2) is enabled directly from the RTG voltage sensor during peak load time rather than through power transistors between the battery cells and the LIVC, as is done in the present discrete component system.

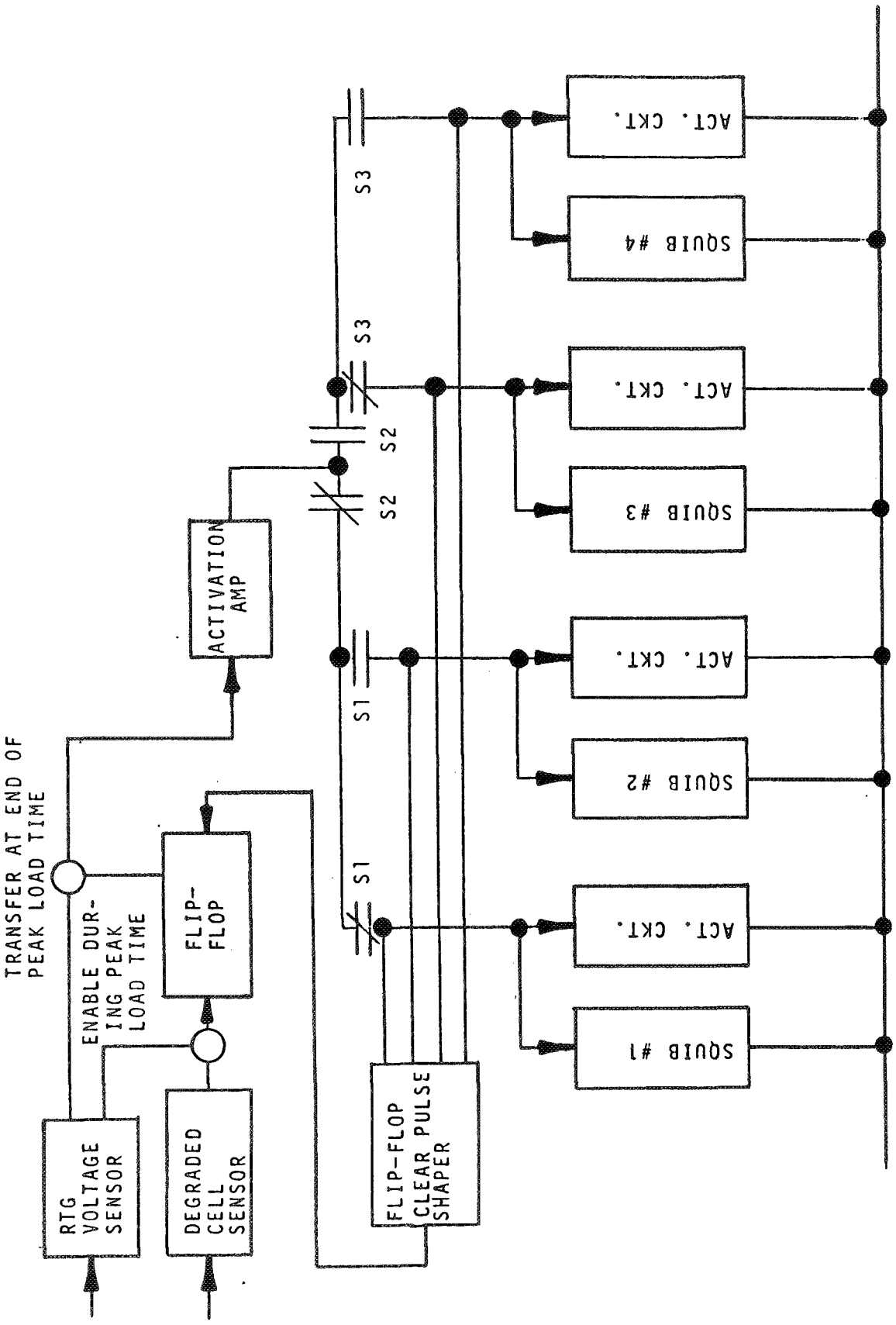


Figure 41. Squib Switch Charge and Discharge Controls

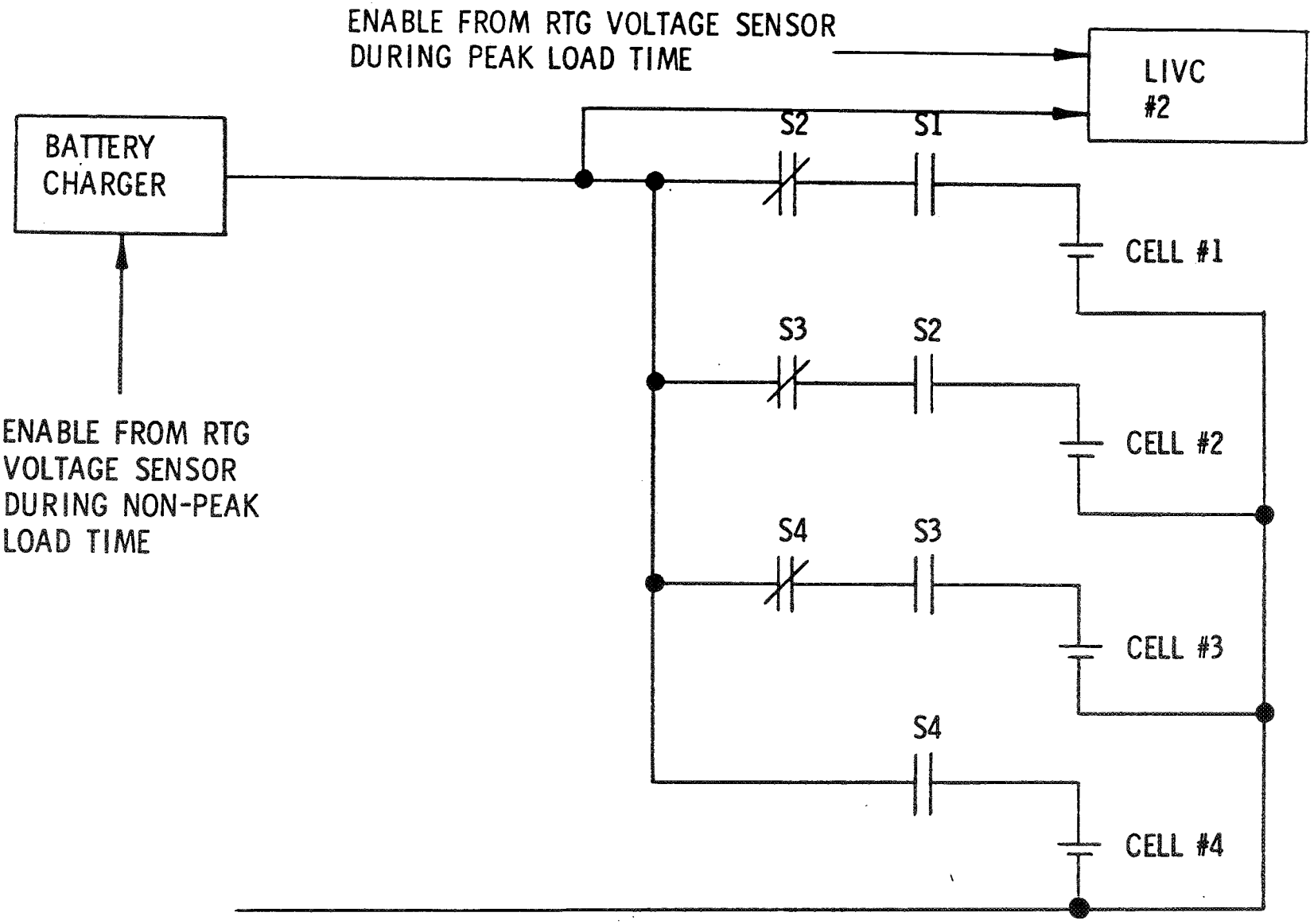


Figure 42. Squib Switch Battery Sequencing Circuit

2. Reliability

Reliability predictions have been prepared for three configurations of the LIVCR System:

1) The single-channel system presently under development.

2) A system employing majority voting by a triple redundant configuration of the converter, regulator, and sensing portions of the circuits.

3) A system employing OR logic circuitry which will allow the system to operate if one of triple redundant configurations (converter, regulator, and sensors) is operating.

Allocations were prepared for both MIL-STD and high-reliability component usage and also with and without considering the reliability of the RTG source and the cell. In all cases, the reliability estimate was made with the charge and discharge control circuits (and the cell activation circuits and cell where applicable) considered to be in the standby redundancy mode of operation.

In the triple-redundant systems, a majority-vote logic circuit and an OR logic circuit were included to process signals from the sequencing circuits in selecting the cell activation circuits and the cell which are to be operational at a given time.

With these considerations, estimates indicate the following three-year reliability for the configurations considered:

- Single-System
  - Source and cell excluded:

    Reliability using MIL-STD parts: $R = 0.012$

    Reliability using Hi-Rel parts: $R = 0.733$

- Source and cell included

  Reliability using MIL-STD parts: R = 0.011

  Reliability using Hi-Rel parts: R = 0.660

- Triple-redundant system, majority-vote logic for cell control and selection

  - Source and cell excluded

    Reliability using MIL-STD parts: R = 0.00045

    Reliability using Hi-Rel parts: R = 0.816

  - Source and cell included

    Reliability using MIL-STD parts: R = 0.0003

    Reliability using Hi-Rel parts: R = 0.724

- Triple-redundant system, OR logic for cell control and selection

  - Source and cell excluded

    Reliability using MIL-STD parts: R = 0.2939

    Reliability using Hi-Rel parts: R = 0.9707

  - Source and cell included

    Reliability using MIL-STD parts: R = 0.2650

    Reliability using Hi-Rel parts: R = 0.9504

In obtaining the reliability estimate for the triple-redundant system employing OR logic circuitry, the reliability of triple-redundant converter, regulator, and sensor circuitry was computed using parallel redundancy principles. This value and the reliability estimate for the charge and discharge control and cell activation and cell circuits considered in standby-redundancy were used to calculate the reliability of OR logic circuitry necessary to obtain a total system reliability of 0.950. The reliability of the OR logic circuitry must surpass a minimum of 0.9895 to obtain a total system reliability of 0.950.

This analysis was conducted based on parts populations and, inasmuch as a firm reliability goal has not as yet been established, will serve as a guide toward adjusting reliability of the system subsections and achieving the required reliability goal. It is anticipated that the required goal will be in the vicinity of 0.95 to 0.99 for the three-year mission, so that the following preliminary conclusions can be stated:

The use of high-reliability parts will be required.

Complex (probably triple) redundancy employing OR logic circuitry for cell control and selection will be needed to achieve the required reliability.

The LIVCR configurations shown in Figures 43, 44, and 45 were analyzed to estimate apportionment of reliability among the system subsections. In the analysis, a probable parts population count was first made, based on the present system configuration, for each functional electronic circuit section. These data are tabulated in Table 2, together with the estimated component failure rate, total circuit failure rate, and three-year operating reliability. The following assumptions were made in calculating the failure rate data of this table:

a. General

1. The exponential probability function is applicable.

2. The failure of any component within a circuit section consitutes failure of the circuit without consideration given to failure mode.

b. MIL-STD Parts

1. Failure rate data presented in MIL-HDBK 217A were used.
2. The ground application factor was applied in all cases.

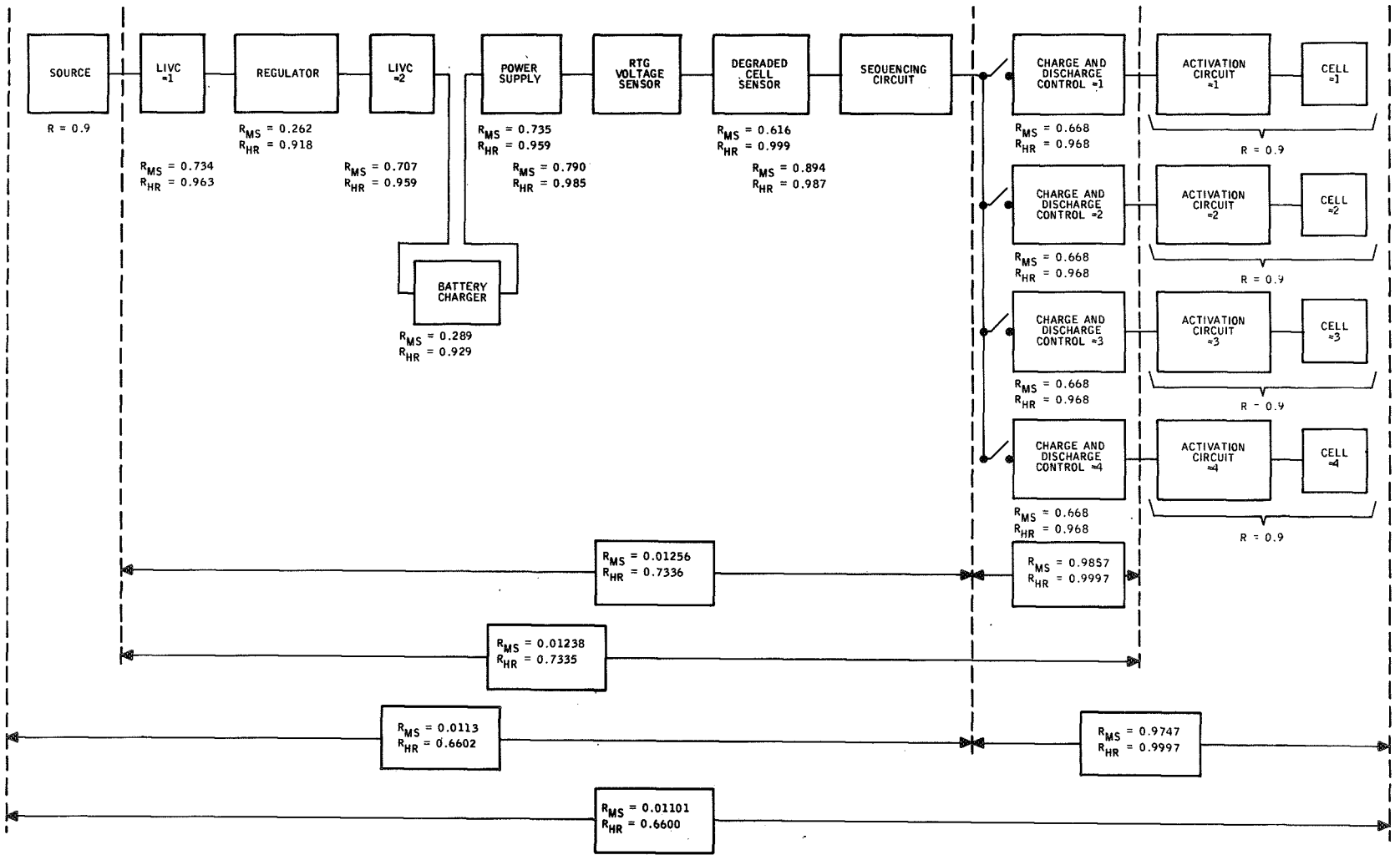
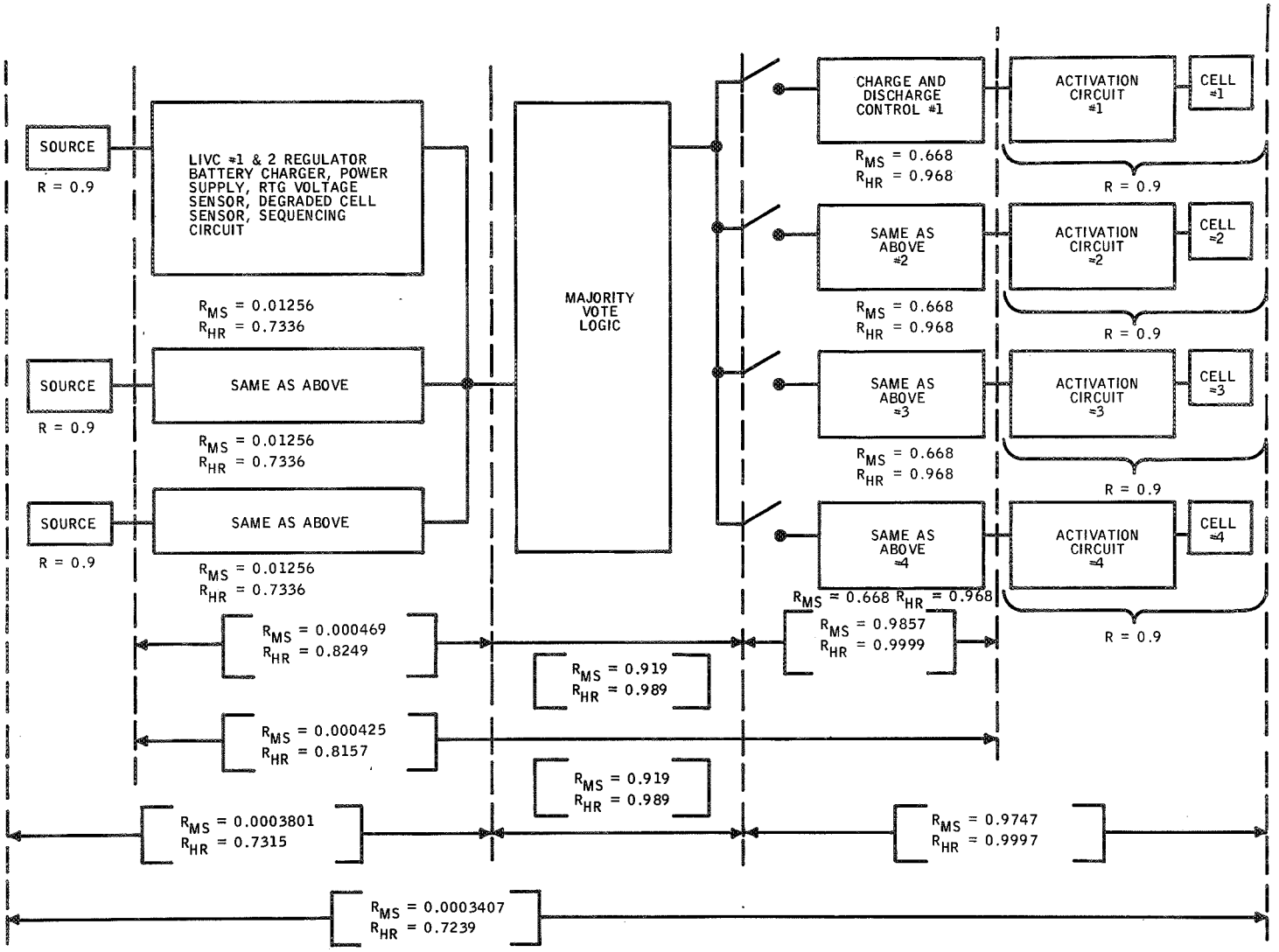
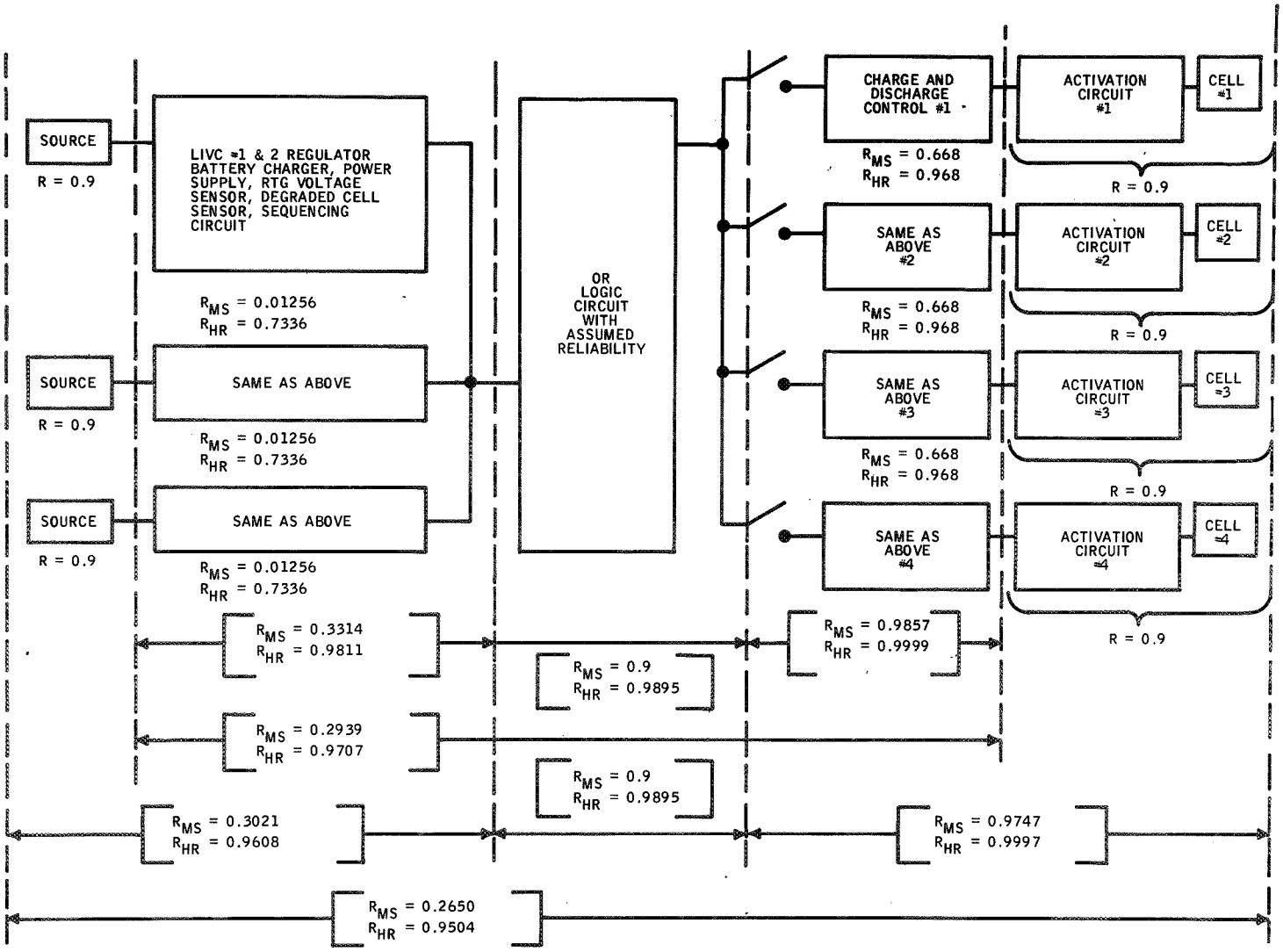


Figure 43. Reliability Allocation LIVC Single System



R_{MS} = RELIABILITY FOR 3 YR. MISSION USING MIL-STD-PARTS.
R_{HR} = RELIABILITY FOR 3 YR. MISSION USING HIGH RELIABILITY PARTS.

Figure 44. Reliability Allocation LIVC Redundant System



R_{MS} = RELIABILITY FOR 3-YR MISSION USING MIL-STD-PARTS.
R_{HR} = RELIABILITY FOR 3-YR MISSION USING MIL-STD-PARTS.

Figure 45. Reliability for 3-Year Mission

TABLE 2. Failure Rate Data

CIRCUIT/COMPONENT	NO.	MIL-HDBK-217A		APOLLO 50 C	
		PART FAILURE RATE PER 10^6 HOURS	TOTAL FAILURES PER 10^6 HOURS	PART FAILURE RATE PER 10^6 HOURS	TOTAL FAILURES PER 10^6 HOURS
CIRCUIT: LIVC NO. 1					
TRANSFORMER	2	1.050	2.100	0.500	1.000
INDUCTOR, SIGNAL	1	1.050	1.050	0.100	0.100
TRANSISTOR, POWER, GE PNP	2	1.950	3.900	0.100	0.200
TRANSISTOR, SIGNAL, S1 NPN	1	1.487	0.487	0.020	0.020
SILICON-CONTROLLED RECTIFIER	1	1.380	1.380	0.020	0.020
DIODE SIGNAL	4	0.487	1.948	0.0075	0.030
RESISTOR FILM	7	0.063	0.441	0.006	0.042
CAPACITOR, TANTALUM	1	0.480	0.480	0.020	0.020
TOTAL FAILURE RATE			11.786		1.432
RELIABILITY FOR 3-YEAR MISSION			0.734		0.963
CIRCUIT: LIVC NO. 2					
TRANSFORMER	2	1.050	2.100	0.500	1.000
INDUCTOR, SIGNAL	2	1.050	2.100	0.100	0.200
TRANSISTOR, POWER, GE PNP	2	1.950	3.900	0.100	0.200
TRANSISTOR, SIGNAL, S1 NPN	1	0.487	0.487	0.020	0.020
RESISTOR, FILM	5	0.063	0.315	0.006	0.030
RESISTOR, WIRE-WOUND	4	0.240	0.960	0.007	0.028
DIODE, SIGNAL	2	0.487	0.974	0.0075	0.015
CAPACITOR, TANTALUM	2	0.480	0.960	0.020	0.040
SILICON-CONTROLLED RECTIFIER	1	1.380	1.380	0.020	0.020
TOTAL FAILURE RATE			13.176		1.553
RELIABILITY FOR 3-YEAR MISSION			0.707		0.959
CIRCUIT: REGULATOR					
INDUCTOR, POWER	1	1.050	1.050	0.100	0.100
TRANSISTOR, POWER, GE PNP	2	1.950	3.900	0.100	0.200
TRANSISTOR, UNIJUNCTION	2	0.487	0.974	0.010	0.020
TRANSISTOR, SIGNAL, S1 PNP	2	0.920	1.840	0.020	0.040
TRANSISTOR, SIGNAL, S1 NPN	8	0.487	3.896	0.020	0.160
DIODE, POWER	11	0.930	10.230	0.050	0.550
DIODE, SIGNAL	8	0.487	3.896	0.020	0.160
DIODE, ZENER	6	0.980	5.880	0.030	0.180
SILICON-CONTROLLED RECTIFIER	3	1.380	4.140	0.020	0.060
RESISTOR, FILM	35	0.063	2.205	0.006	0.210
POTENTIOMETER	2	3.820	7.640	0.100	0.200
CAPACITOR, TANTALUM	6	0.480	2.880	0.020	0.120
CAPACITOR, GLASS	9	0.011	0.099	0.004	0.036
CAPACITOR, ALUMINUM	1	0.037	0.037	0.020	0.020
RESISTOR, WIRE-WOUND	1	0.240	0.240	0.007	0.007
TRANSFORMER	2	1.050	2.100	0.500	1.000
TOTAL FAILURE RATE			51.007		3.063
RELIABILITY FOR 3-YEAR MISSION			0.262		0.918
CIRCUIT: RTG VOLTAGE SENSOR					
TRANSISTOR, SIGNAL, S1 NPN	1	0.487	0.487	0.020	0.020
TRANSISTOR, POWER, GE PNP	3	1.950	5.850	0.100	0.300
DIODE, SIGNAL	3	0.487	1.461	0.020	0.060
RESISTOR, FILM	10	0.063	0.630	0.006	0.060
CAPACITOR, GLASS	3	0.011	0.033	0.004	0.012
CAPACITOR, ALUMINUM	3	0.037	0.111	0.020	0.060
INTEGRATED CIRCUIT 2 GATES 1/2 S/N 5400	0.5	0.800	0.400	0.100	0.050
TOTAL FAILURE RATE			8.972		0.562
RELIABILITY FOR 3-YEAR MISSION			0.790		0.985

TABLE 2. Failure Rate Data (Concluded)

CIRCUIT/COMPONENT	NO.	MIL-HDBK-217A		APOLLO 50 C	
		PART FAILURE RATE PER 10^6 HOURS	TOTAL FAILURES PER 10^6 HOURS	PART FAILURE RATE PER 10^6 HOURS	TOTAL FAILURES PER 10^6 HOURS
CIRCUIT: DEGRADED CELL SENSOR					
TRANSISTOR, POWER, GE PNP	4	1.950	7.800	0.100	0.400
DIODE, SIGNAL	3	0.487	1.462	0.0075	0.0225
DIODE, ZENER	3	0.980	2.940	0.030	0.090
RESISTOR, FILM	10	0.063	0.630	0.006	0.060
POTENTIOMETER	1	3.820	3.820	0.100	0.100
CAPACITOR, TANTALUM	1	0.480	0.480	0.020	0.020
SILICON-CONTROLLED RECTIFIER	1	1.380	1.380	0.020	0.020
TOTAL FAILURE RATE			18.511		0.712
RELIABILITY FOR 3-YEAR MISSION			0.616		0.999
CIRCUIT: SEQUENCING CIRCUIT					
RESISTOR, FILM	1	0.063	0.063	0.006	0.006
SWITCH, TOGGLE	1	0.100	0.100	0.001	0.001
INTEGRATED CIRCUIT, CD2203	4	0.800	3.200	0.100	0.400
INTEGRATED CIRCUIT 2 GATES 1/2 S/N 5400	0.5	0.800	0.400	0.100	0.050
DIODE, SIGNAL	1	0.487	0.487	0.020	0.020
CAPACITOR, GLASS	1	0.011	0.011	0.004	0.004
TOTAL FAILURE RATE			4.261		0.481
RELIABILITY FOR 3-YEAR MISSION			0.894		0.987
CIRCUIT: POWER SUPPLY					
TRANSFORMER	2	1.050	2.100	0.500	1.000
TRANSISTOR, POWER, S1 NPN	2	0.650	1.300	0.177	0.354
DIODE, SIGNAL	8	0.487	3.896	0.0075	0.060
DIODE, ZENER	2	0.980	1.960	0.030	0.060
RESISTOR, WIRE-WOUND	1	0.240	0.240	0.007	0.007
RESISTOR, FILM	5	0.063	0.315	0.006	0.030
CAPACITOR, TANTALUM	4	0.480	1.920	0.020	0.080
TOTAL FAILURE RATE			11.731		1.591
RELIABILITY FOR 3-YEAR MISSION			0.735		0.959
CIRCUIT: BATTERY CHARGER					
TRANSFORMER, SIGNAL	1	1.050	1.050	0.500	0.500
INDUCTOR, POWER	1	1.050	1.050	0.100	0.100
TRANSISTOR, POWER GE PNP	8	1.950	15.600	0.100	0.800
TRANSISTOR, SIGNAL S1 PNP	3	0.487	1.461	0.020	0.060
UNIJUNCTION, TRANSISTOR	2	0.487	0.974	0.010	0.020
TRANSISTOR, POWER S1 NPN	1	0.650	0.650	0.177	0.177
TRANSISTOR, SIGNAL S1 NPN	3	0.920	2.760	0.020	0.060
DIODE, SIGNAL	14	0.487	6.818	0.020	0.280
DIODE, ZENER	4	0.980	3.920	0.030	0.120
RESISTOR, FILM	46	0.063	2.898	0.006	0.378
POTENTIOMETER	2	3.820	7.640	0.100	0.200
CAPACITOR, TANTALUM	5	0.480	2.400	0.020	0.100
CAPACITOR, GLASS	2	0.011	0.022	0.004	0.008
TOTAL FAILURE RATE			47.243		2.803
RELIABILITY FOR 3-YEAR MISSION			0.289		0.929
CIRCUIT: CHARGE & DISCHARGE CONTROL (EACH OF 4 CIRCUITS)					
TRANSISTOR, POWER S1, PNP	2	0.975	1.950	0.100	0.200
TRANSISTOR, POWER GE PNP	5	1.950	9.750	0.100	0.500
RESISTOR, FILM	7	0.063	0.421	0.060	0.420
RESISTOR, WIRE-WOUND	3	0.240	0.720	0.007	0.021
DIODE, SIGNAL	5	0.487	2.335	0.0075	0.0375
INTEGRATED CIRCUIT 2 GATES 1/2 S/ N 5400	0.250	0.800	0.200	0.100	0.025
TOTAL FAILURE RATE			15.396		1.203
RELIABILITY FOR 3-YEAR MISSION			0.668		0.968
CIRCUIT: MAJORITY VOTE LOGIC					
INTEGRATED CIRCUIT S/N 5454	4	0.800	3.200	0.100	0.400
RELIABILITY FOR 3-YEAR MISSION			0.919		0.989

3. Transistors and diodes – normalized junction temperature was estimated at 0.4, approximating a device dissipating 10 percent power at an ambient of 50°C.

4. Silicon-controlled rectifiers – data given for a Si pnp transistor was used.

5. Unijunction Transistor – data given for a Si npn transistor was used.

6. Wire-wound resistors and potentiometers – assumed to dissipate 50 percent rated wattage at 50°C ambient. Wire-wound resistors assumed to be used for resistances less than 10 ohms.

7. Film resistors – assumed to dissipate 20 percent rated wattage at 50°C ambient. Assumed to be used for resistances greater than 10 ohms.

8. Solid tantalum and aluminum capacitors – assumed to be stressed at 50 percent rated voltage at 50°C ambient. Tantalum assumed for $C \geq 22\ \mu f$.

9. Glass capacitors – assumed to be stressed at 10 percent rated voltage at 50°C ambient. Assumed to be used for capacitances less than $1\ \mu f$.

10. Transformers and coils – MIL-T-27 units utilizing Class Q insulation and at a maximum operating temperature of 85°C.

11. Integrated circuits – Estimate of realistic failure for this reliability-level part based on vendor data.

c. High-Reliability Parts

1. Failure rates are those applied by Honeywell to the Apollo program and were established from the Minuteman Handbook, vendor data, and other sources.

   References: Honeywell Interoffice Memo from S. A. Bastiem to J. N. Mitchell, dated 17 December 1964, Subject: Updated Apollo Failure Rates.

2. Integrated Circuits – Estimate of realistic failure rate for high-reliability integrated circuits based on vendor-supplied data and other sources.

In the allocations of Figures 43, 44, and 45, the estimates were made for the systems, both excluding and including RTG source, activation circuit, and cell reliability considerations. A three-year reliability of 0.9 for both the source and activation circuit-cell combination was assumed. No further consideration was made to differentiate between the storage and operating failure rates for these components in these approximations.

In calculating the reliability of the charge and discharge control circuits (and the cell activation circuits and cells, where applicable), the principles of active-standby redundancy were applied. These account for operation, beginning with one active unit and sequentially switching in a standby unit upon sensing failure of the previously active unit. The system under consideration is a 1 + 3 system (one active and three standby units). The general equation for the reliability of a 1 + N system is as follows:

$$R_{1+N} = \sum_{n=0}^{N} \left(\frac{n+\alpha-1}{n}\right) B^n (1-B)^{\alpha}$$

where $B = 1 - e$

$\alpha = M \left(\frac{\lambda o}{\lambda s}\right)$

M = number of active units

N = number of standby units at start of mission

λo, λs = operating and standby mode failure rates respectively, per hour

t = mission time, hour

The majority-vote logic circuit used in the redundant system is shown in Figure 46. This circuit selects the cell activation circuit and cell as indicated by the majority of the sequencing circuit signals. The circuit is anticipated to require a total of 16 gates (four integrated circuit chips), shown in the figure. The following equation is used to determine the reliability of this system:

$$R_S = R^3 + 3R^2Q$$

where Rs = system reliability

R = element reliability

Q = element unreliability = 1 - R

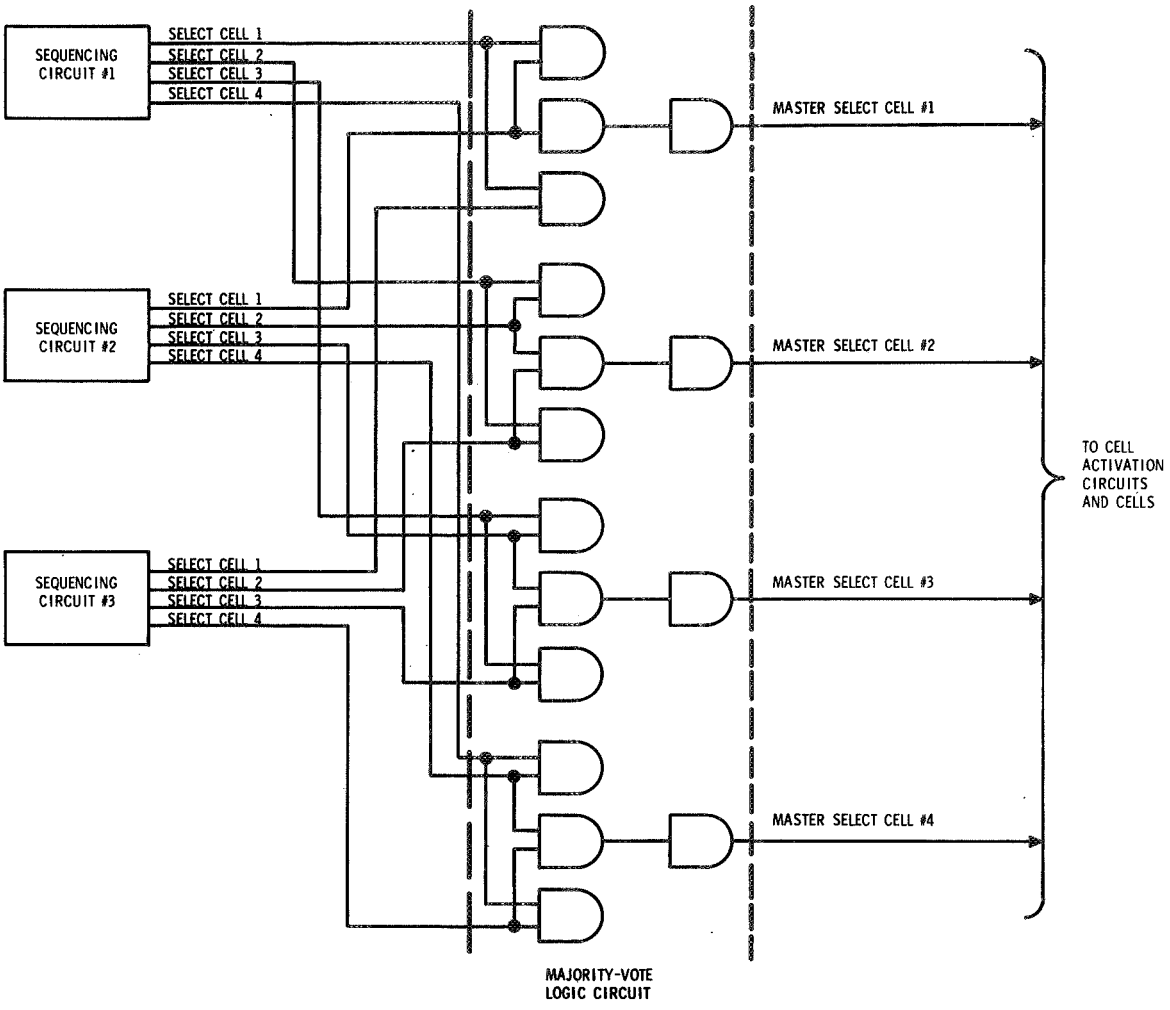


Figure 46. Cell Selection Majority Vote Logic Circuit

II. ALTERNATE RTG SOURCE CONSIDERATIONS

The present system has been designed to use two SNAP-19 RTG's in parallel as a primary power source. This combination provides 66 watts at 3 volts and 22 amperes. Consideration has been given to using a SNAP-27 RTG. A single SNAP-27 RTG will provide a maximum power output of 50 watts at 14 volts. The considerations and comments given here are, strictly, results of a paper work study. There was no hardware of any kind constructed or tested to interface with a power source with the SNAP-27 characteristics. The study has been made for a system with the same power output requirements. These requirements makes it necessary to consider the use of two SNAP-27 RTG's in parallel. This is necessary even though higher energy batteries may be used. The approximate 10 watts to charge the battery, plus the maximum nonpeak load of 45 watts, adds up to more than maximum 50-watt output of one RTG. With two RTG's in parallel the power supply characteristics are 100 watts at 14 volts, 7.14 amperes, and 1.96 ohms. It should be noted here that the internal impedance of this RTG apparently varies slightly with current. However, because the exact impedance variation is not known and to simplify the study, the internal impedance is assumed to be that calculated for 50 watts at 14 volts which is 3.92 ohms.

The inverter design for this power source would be somewhat different than the final design used in the present system. The main reason for this is that in the present design the inverter transistor-driven current gain is very nearly equal to the turns ratio of the power output transformer. In the present design this turns ratio is 14.7, and a driven Beta of 14.7 is satisfactory for efficient operation of the transistors used in the inverter. The transformer turns ratio using the SNAP-27 RTG's would be about 3, and a driven Beta of 3 is not practical for known transistors that might be used for this application. Using secondary current as a source for inverter drive is most desirable, and this can be accomplished by using current sensing windings on the inverter transistors base drive transformers.

These windings will be placed in series with the output lines of the output transformer and will act as the primary windings for the base drive transformer. This method of using secondary current for inverter drive was suggested by NASA* and has been proven to be very effective and efficient.

The RTG short circuit current is approximately 14.5 amperes. The transistors (2N2832) used in the present LIVC are rated at 20 amperes maximum. This means that 1 transistor (instead of 3 as used in the present design) can be used in each side of the inverter. This one transistor would conduct about 7.14 amperes under maximum load conditions. This is about the same as one transistor carries in the present system. This means that the power loss in the inverter transistors would be about one third that in the present system.

It might be necessary to increase the size of the core of the power output transformer. This is because the input voltage is higher. The core area could be kept the same by increasing the number of primary turns by 3. It would be necessary to decrease the wire size to accommodate the larger number of turns. This, along with the increase in total length of the primary, would increase the primary resistance. If the resistance goes up by 7 times (2 times for smaller wire and approximately 3.5 times for increased length), the overall I^2R loss in the primary would go down because the current is decreased by a factor of 3. The decrease in primary winding I^2R loss would be to approximately $7/3^2$ or 7/9 of the original losses. This will be partially offset by the increase in secondary I^2R loss. The secondary current will remain the same, but the resistance will increase because the number of secondary turns will; the length of wire will increase by approximately 3.5 times and it will be necessary to reduce the size of the wire to accommodate the increased number of turns (assuming the same size core is used). We can assume that the resistance may increase at least 7 times. An extra loss will occur in this approach. This loss is created by the transistor base voltage reflected into the secondary from the transistor base drive transformer. The base saturation voltage is nominally 0.55 volts.

*NASA Report No. X-716-68-49 by E.R. Pasciutti.

The turns ratio in the feedback will be about 3. The voltage reflected into the output will be 0.55/3 or 0.18 volts. The output current at maximum load at this point in the circuit is about 1.5 amperes. The power loss seen from this source is 1.5 X 0.55 or 0.825 watt. Another source of power loss in the LIVC is in the rectifier diodes in the output. This loss will be the same for either system and is approximately 1.8 watts. The total calculated losses for this system (using calculated values for the old system) would be total transistor losses + primary losses + secondary losses which equals 4.38/3 + 0.0259 X 6 + 0.5 X 2/3 + 0.825 + 1.8 = 1.46 + 0.1554 + 0.33 + 0.825 + 1.8 = 4.57 watts. This gives an LIVC efficiency of about 93 percent as compared to 91 percent for the present system.

The computer program was run using the assumed parameters of the SNAP-27 RTG. Computer print-out number 2 (page I-5 in Appendix I) shows that the optimum turns ratios for minimum battery current is 3.6 for the RTG LIVC and 35 for the battery LIVC. The battery current for a 135-watt load is 40.83 amperes. This run was made with a 93 percent efficiency for the RTG LIVC and 84.5 percent efficiency for the battery LIVC. It was assumed that the battery LIVC would operate at a greater efficiency at this current level so another run was made using an efficiency of 87 percent. The results of this run are shown in computer print-out number 2 (page I-6 in Appendix I). The battery current decreased to 39.3 amperes. The RTG LIVC turns ratios were not varied as much for this run because the previous run showed that the optimum RTG LIVC turns ratio is about 3.6.

The computer program was run several times with increasing power output levels. It was found that with two SNAP-27 RTG's in parallel a power output of 190 watts would draw about the same battery current (approximately 74 amperes) as the present system does with a 150-watt load. The 190-watt and 150-watt figures are the power levels at the input to the regulator. Assuming a 90 percent regulator efficiency these figures represent power outputs of 171 watts or 135 watts, respectively. The computer print-out for the 190-watt load is shown in Computer Print-out number 4 (page I-6 of Appendix I).

It appears that if the weight and volume of two SNAP-27 RTG's are acceptable, a system using this type source is more desirable. Smaller batteries could be used, and this would compensate in part or possibly for all the weight and volume increase contributed by the larger RTG's. One problem with the present design is that with the efficiencies obtained there is not quite enough power available from the SNAP-19's to maintain a 45-watt output load and charge the batteries completely at a 5-ampere rate. Using two SNAP-27's would more than eliminate this problem. The whole system could be scaled to a higher output load simply by modifying the RTG LIVC.

III. SCALING UP TO HIGHER POWER

No specifications were given for the amount of increase in power levels. Although there was not a large effort expended for this study, there have been some observations made in the course of developing the breadboard for the contract. These have led to some conclusions about upgrading power levels of this type of system.

As explained in Section II, the power output level can be raised to 170 watts simply by using two SNAP-27 RTG's as a primary source and modifying the RTG LIVC slightly. The output regulator and line switch in the present system are capable of handling this output power without any modification. The line switch consists of two 2N2834 transistors in parallel. These transistors are capable of carrying 20 amperes each. The purpose of using two of these transistors is to improve the regulator efficiency and to be able to accommodate the surge currents which occur when the output filter capacitor charges on initial regulator turnon. It may be necessary to increase the size of the output choke to accommodate larger wire and maintain regulator efficiency. The output ripple on the present system is approximately 40 millivolts peak-to-peak. A larger choke would reduce this ripple.

It is estimated the power switching portion of the output regulator can handle at least twice the power requirements of the present system. This would be 270 watts. It may be necessary to redesign the current drive transformers to prevent core saturation at the higher current level. One limitation to the present regulator is the input voltage level that will occur at low loads. It will be necessary to increase the LIVC output transformer turns ratios somewhat to ensure sufficient voltage at the input to the regulator for proper regulation at high loads. The voltage level itself is not a real problem because components can be obtained with high enough voltage ratings to withstand a moderate increase in voltage at this point.

The big problem is the current surge that occurs when the regulator power switching transistor turns on. The capacitor on the input to the regulator charges to the no load voltage during initial turnon. The charged capacitor is an extremely low-impedance source and the output filter capacitor is a very low-impedance load when the switching transistor first turns on. The output filter choke does limit the current momentarily, but experience has shown that the switching transistor will fail when the input voltage is allowed to get above 75 volts. Examination of the transistors that failed showed that they all failed because of excess current.

It appears that for any load requirements of more than 270 watts other design changes must be considered. Unless the output requirements are increased by a very large amount, the present LIVC designs can be used for increased power requirements. All that is necessary is to put more transistors in parallel or use higher power transistors. The problems and limitations of paralleling a large number of power transistors are very well known and will not be discussed here.

Another method of scaling up the power is to parallel portions of the system or the complete system. If paralleled LIVC's are used, the weight and volume may be greater than it would be in just paralleling transistors in one LIVC. This is because it may be necessary to use separate output transformers for each LIVC. It is possible to use separate primaries on one output transformer. If this is done a synchronizing system must be used to ensure that all the transistors switch in the proper phase. Synchronizing circuits have been studied and discussed in previous contracts, but no effort has been made during this contract period to determine whether or not these approaches can be adapted for the present LIVC design.

IV. NEW TECHNOLOGY

The only development during the final quarter that can be considered as new technology is the new method used to sense current in the battery charger circuit. The transformer used for sensing the charging current is inserted in the charging line. Current is sensed during the "on time" of the series switch. The transformer core is reset by the freewheeling current which occurs during the "off time." This development is discussed in the section covering the battery charger. The transformer connection is similar to that used in the current drive transformer in the output regulator. The following is a list and location of new technology developed during this contract period.

1. 90-Watt LIVC, Section 1, Paragraph 3, 2nd Quarterly Report.
2. Current Sensor, Section 1, Paragraph c, 3rd Quarterly Report.
3. Voltage Regulator, Section 1, Paragraph g, 3rd Quarterly Report.
4. Composite Core Technique, Section 1, Paragraph e, 3rd Quarterly Report.
5. Inverter Circuit, Section 1, Paragraph a, 4th Quarterly Report.
6. Inverter Starting Circuit, Section 1, Paragraph b, 5th Quarterly Report.
7. Current Drive Circuit, Section 1, Paragraph f, 6th Quarterly Report.
8. Voltage Sensing Circuit, Section 1, Paragraph e, 7th Quarterly Report.

V. CONCLUSIONS AND RECOMMENDATIONS

The final breadboard system comes fairly close to meeting the desired specifications. The output ripple is somewhat higher than desired. The maximum ripple requested was 25 millivolts peak-to-peak. The breadboard has a maximum of 40 millivolts peak-to-peak. This ripple can easily be reduced by using a larger output filter capacitor, a larger filter choke, or a combination of both.

The system efficiency is not quite high enough to charge the batteries at a 5-ampere rate and maintain a 45-watt output load. This problem can be eliminated by using two SNAP-27 RTG's in parallel as a primary source rather than two SNAP 19 RTG's. It is recommended that the SNAP-27 be considered over the SNAP-19 for this application. Another advantage to using the SNAP-27 RTG is that the battery drain is less at maximum loads (approximately 40 amperes). This makes it possible to use much smaller batteries in the system. It also reduces the requirements of the battery discharge circuit and the battery LIVC. The number of transistors in both circuits can be reduced by 0.5. This eliminates six 50-ampere transistors. There would also be four 20-ampere transistors eliminated in the RTG LIVC. Elimination of these transistors would increase the system efficiency and reduce cooling problems.

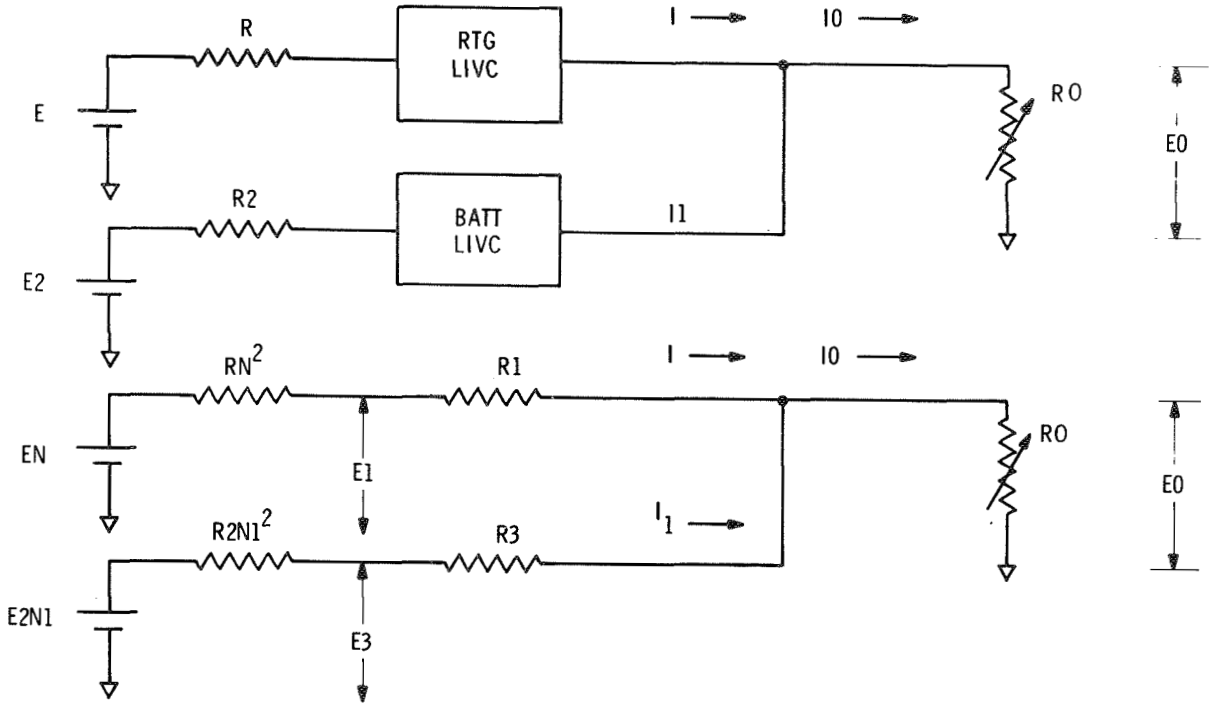
Another very important advantage to using the SNAP-27 is that it becomes practical to perform RTG voltage-limiting at the output of the RTG. If the limiting is done at this point a single filter could be used at the output of the voltage limiter to provide a relatively smooth D.C. voltage for system operation. This is a very important point because considerable problems were encountered in the original system design due to the extreme voltage transients imposed on the system when the overvoltage circuit was operating.

Use of SNAP-27 RTG's would also permit scaling up the system to higher power capabilities with very little system design change. This is covered in greater detail in Section II.

Another development that should be considered seriously for future designs is the use of squib switches in portions of the logic switching. There are two distinct advantages in this approach: One is that the efficiency would be higher in the battery charge and discharge system. The other is that this approach provides a memory in the logic and sequencing circuits. There should also be fewer parts; however, this does not necessarily mean a reduction in weight and volume, because squib switches for these power levels can be quite bulky.

One disadvantage to using squib switches is that because they are a "one-shot" device it would be difficult to check the system logic. In a breadboard system this problem could be overcome by using some form of latching relay to simulate the squib switch. Another disadvantage is that there is no way to recycle or reset the logic or switching sequence if inadvertent sequencing occurs in actual operation.

APPENDIX I



DEVELOPMENT OF EQUATIONS FOR PROGRAM WOL

$S = RN2+R1,\ T = R2N1^2 + R3,\ G1 = 1/S;\ G2 = 1/T,\ G0 = 1/RO$

$(G1 + G2 + G0)\ E0 - ENG1 - E2N1G2 = 0$

$$EO = \frac{EN\,G1 + E2\ N1G2}{G1 + G2 + G0} = \frac{EN/S + E_2\,N1/T}{1/S + 1/T + 1/R0}$$

$$EO = \frac{(ENT + E2N1S)RO}{TR0 + SR0 + ST},\quad I = \frac{(EN - EO)}{(RN\,2 + R1)}$$

$$I1 = \frac{(E2N1 - E0)}{(R2N1^2 + R3)},\quad I2 = NI,\quad I3 = N1I1$$

DEVELOPMENT OF EQUATIONS FOR PROGRAM VIC

$$E2N1 = I1R2N1^2 + E3; \quad I1R2N1^2 - E2N1 + E3 = 0$$

$$N1 = \frac{E2 \pm (E2^2 - 4I1R2E3)^{1/2}}{2I1\ R2}$$

A1 = RTG efficiency at RTG peak power ÷ 100 = .5

A2 = RTG LIVC efficiency ÷ 100

A3 = Battery LIVC efficiency ÷ 100

I = RTG LIVC Secondary current

I1 = Battery LIVC Secondary current

I2 = RTG current

I3 = Battery current

IQ = Load current

E = RTG Voltage

E1 = Output voltage of lossless RTG LIVC

E2 = Battery voltage

E3 = Output voltage of lossless battery LIVC

E0 = Output voltage (input voltage to regulator)

R = RTG resistance

R1 = Resistance representing RTG LIVC losses

R2 = Battery resistance

R3 = Resistance representing battery LIVC losses

R0 = Output resistance at 150 watts load

N = Turns ratio of RTG LIVC output transformer

N1 = Turns ratio of battery LIVC output transformer

```
?LIST VIC


20 PRINT"E    E2    A1    A2    A3    N    I2    P    R    R2"
21 INPUT E,E2,A1,A2,A3,N,I2,P,R,R2
30 E0=E*A1*A2*N
40 I=I2/N
50 I0=P/E0
60 I1=I0-I
69 E3=E0/A3
70 N1=(E2-(E2↑2-4*R2*I1*E3)↑(.5))/(2*R2*I1)
71 I3=I1*N1
80 E1=E0/A2
90 R1=(E1-E0)/I
110 R3=(E3-E0)/I1
119 PRINT "        E0             I3             R3             R1             N1"
120 PRINT,130,E0,I3,R3,R1,N1
130 FMT E13.6,E13.6,E13.6,E13.6,E13.6
135 CALL W0L
140 END


?LIST W0L


1 PRINT " X      Y      Z      A      B      C"
2 INPUT X,Y,Z,A,B,C
5 PRINT TAB(7) "I2" TAB(20) "I3" TAB(33) "E0" TAB(44) "N1" TAB(54),
6 PRINT TAB(54) "P" TAB (64) "R0"
10 F0R N=X,Y,Z
11 PRINT,12,N
12 FMT "N=",F6.2
20 F0R N1=A,B,C
25 F0R R0=12,7,-.01
30 S=.136*N↑2+R1
40 T=.002*N1↑2+R3
50 E0=((E*N*T+E2*N1*S)*(R0))/(T*R0+S*R0+S*T)
55 P=E0↑2/R0
60 I=(E*N-E0)/(R*N↑2+R1)
70 I1=(E2*N1-E0)/(R2*N1↑2+R3)
80 I2=I*N
90 I3=I1*N1
92 IF P>150 THEN 100
93 NEXT R0
100 PRINT,110,I2,I3,E0,N1,P,R0
110 FMT E13.6,E13.6,E13.6,X2,F6.2,E13.6,X1,F6.2
120 NEXT N1
130 PRINT,140,I2,I3,E0,N1,P,R0
140 FMT E13.6,E13.6,E13.6,X2,F6.2,E13.6,X1,F6.2
150 NEXT N
160 RETURN
```

```
 BASIC VIC
RUN
E   E2   A1   A2   A3   N   I2   P   R   R2
!6,1.6, .5, .91,  .845,14.7,22,150,.136,.002
       E0            I3            R3            R1            N1
  .401310E 02   .732264E 02   .328460E 01   .265202E 01   .326734E 02
 X     Y     Z     A     B     C
!13,  15,   .5,   33,   36,   .5
      I2            I3            E0            N1            P            R0
N= 13.00
  .189797E 02   .738705E 02   .405720E 02   33.00   .150055E 03   10.97
  .185190E 02   .734298E 02   .414806E 02   33.50   .150013E 03   11.47
  .180735E 02   .731502E 02   .423591E 02   34.00   .150025E 03   11.96
  .176371E 02   .729596E 02   .432196E 02   34.50   .150036E 03   12.45
  .172091E 02   .728512E 02   .440637E 02   35.00   .150047E 03   12.94
  .167845E 02   .727660E 02   .449010E 02   35.50   .150008E 03   13.44
  .163717E 02   .728070E 02   .457151E 02   36.00   .150027E 03   13.93
  .163717E 02   .728070E 02   .457151E 02   36.50   .150027E 03   13.93
N= 13.50
  .198381E 02   .732166E 02   .406802E 02   33.00   .150036E 03   11.03
  .193883E 02   .727402E 02   .415944E 02   33.50   .150053E 03   11.53
  .189435E 02   .723034E 02   .424985E 02   34.00   .150011E 03   12.04
  .185127E 02   .720202E 02   .433739E 02   34.50   .150024E 03   12.54
  .180903E 02   .718214E 02   .442324E 02   35.00   .150039E 03   13.04
  .176714E 02   .716477E 02   .450839E 02   35.50   .150005E 03   13.55
  .172640E 02   .716017E 02   .459118E 02   36.00   .150028E 03   14.05
  .172640E 02   .716017E 02   .459118E 02   36.50   .150028E 03   14.05
N= 14.00
  .206592E 02   .727859E 02   .407515E 02   33.00   .150018E 03   11.07
  .202148E 02   .722114E 02   .416817E 02   33.50   .150032E 03   11.58
  .197803E 02   .717395E 02   .425913E 02   34.00   .150043E 03   12.09
  .193504E 02   .713048E 02   .434914E 02   34.50   .150001E 03   12.61
  .189334E 02   .710166E 02   .443643E 02   35.00   .150015E 03   13.12
  .185241E 02   .708089E 02   .452211E 02   35.50   .150033E 03   13.63
  .181179E 02   .706245E 02   .460714E 02   36.00   .150005E 03   14.15
  .181179E 02   .706245E 02   .460714E 02   36.50   .150005E 03   14.15
N= 14.50
  .214451E 02   .725657E 02   .407880E 02   33.00   .150016E 03   11.09
  .210059E 02   .718921E 02   .417344E 02   33.50   .150023E 03   11.61
  .205766E 02   .713251E 02   .426595E 02   34.00   .150028E 03   12.13
  .201564E 02   .708560E 02   .435651E 02   34.50   .150033E 03   12.65
  .197445E 02   .704768E 02   .444527E 02   35.00   .150042E 03   13.17
  .193362E 02   .701274E 02   .453325E 02   35.50   .150003E 03   13.70
  .189392E 02   .699102E 02   .461880E 02   36.00   .150023E 03   14.22
  .189392E 02   .699102E 02   .461880E 02   36.50   .150023E 03   14.22
N= 15.00
  .221981E 02   .725458E 02   .407913E 02   33.00   .150040E 03   11.09
  .217637E 02   .717714E 02   .417543E 02   33.50   .150037E 03   11.62
  .213392E 02   .711080E 02   .426952E 02   34.00   .150032E 03   12.15
  .209239E 02   .705465E 02   .436159E 02   34.50   .150028E 03   12.68
  .205170E 02   .700783E 02   .445180E 02   35.00   .150027E 03   13.21
  .201177E 02   .696960E 02   .454030E 02   35.50   .150032E 03   13.74
  .197256E 02   .693934E 02   .462723E 02   36.00   .150044E 03   14.27
  .197256E 02   .693934E 02   .462723E 02   36.50   .150044E 03   14.27

  140 EXIT
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Computer Print-out No. 1

```
?BASIC VEC
RUN
E   E2   A1   A2   A3   N   I2   P   R   R2
!28,1.6,.5,.93,.845,3,7.14,150,1.96,.002
        E0              I3              R3              R1              N1
  .390600E 02   .446831E 02   .490660E 01   .123530E 01   .305997E 02
X  Y  Z  A  B  C
!3.4,3.8,.2,30,35,1
        I2              I3              E0              N1              P              R0
N=  3.40
  .824585E 01   .480702E 02   .372537E 02   30.00   .150043E 03    9.25
  .790740E 01   .452514E 02   .396321E 02   31.00   .150025E 03   10.47
  .760292E 01   .433815E 02   .417718E 02   32.00   .150037E 03   11.63
  .731886E 01   .420709E 02   .437680E 02   33.00   .150014E 03   12.77
  .705139E 01   .412244E 02   .456476E 02   34.00   .150017E 03   13.89
  .679645E 01   .407295E 02   .474391E 02   35.00   .150034E 03   15.00
  .679645E 01   .407295E 02   .474391E 02   36.00   .150034E 03   15.00
N=  3.60
  .865709E 01   .503459E 02   .367450E 02   30.00   .150028E 03    9.00
  .831283E 01   .467944E 02   .392923E 02   31.00   .150042E 03   10.29
  .800514E 01   .443154E 02   .415689E 02   32.00   .150002E 03   11.52
  .772389E 01   .426212E 02   .436499E 02   33.00   .150028E 03   12.70
  .745834E 01   .413791E 02   .456147E 02   34.00   .150017E 03   13.87
  .720579E 01   .405189E 02   .474834E 02   35.00   .150014E 03   15.03
  .720579E 01   .405189E 02   .474834E 02   36.00   .150014E 03   15.03
N=  3.80
  .904610E 01   .533029E 02   .360839E 02   30.00   .150012E 03    8.68
  .869062E 01   .488150E 02   .388472E 02   31.00   .150015E 03   10.06
  .838212E 01   .458052E 02   .412451E 02   32.00   .150018E 03   11.34
  .810139E 01   .436580E 02   .434273E 02   33.00   .150038E 03   12.57
  .783854E 01   .420589E 02   .454704E 02   34.00   .150043E 03   13.78
  .758796E 01   .408290E 02   .474182E 02   35.00   .150001E 03   14.99
  .758796E 01   .408290E 02   .474182E 02   36.00   .150001E 03   14.99

 140 EXIT
```

Computer Print-out No. 2

```
?BASIC VIC
RUN
E    E2    A1    A2    A3    N    I2    P    R    R2
!28,1.6,.5,.93,.87,3,7.14,150,1.96,.002
        E0              I3              R3              R1              N1
  .390600E 02   .433210E 02   .399696E 01   .123530E 01   .296669E 02
X  Y  Z  A  B  C
!3.4,3.6,.2,30,35,1
        I2              I3              E0              N1              P              R0
N=  3.40
  .792651E 01   .439999E 02   .394978E 02   30.00   .150012E 03   10.40
  .764115E 01   .424066E 02   .415031E 02   31.00   .150048E 03   11.48
  .736981E 01   .412381E 02   .434099E 02   32.00   .150037E 03   12.56
  .711015E 01   .404304E 02   .452347E 02   33.00   .150016E 03   13.64
  .686038E 01   .399343E 02   .469899E 02   34.00   .150006E 03   14.72
  .661911E 01   .397107E 02   .486853E 02   35.00   .150019E 03   15.80
  .661911E 01   .397107E 02   .486853E 02   36.00   .150019E 03   15.80
N=  3.60
  .832098E 01   .453757E 02   .392320E 02   30.00   .150019E 03   10.26
  .803692E 01   .432938E 02   .413337E 02   31.00   .150002E 03   11.39
  .777048E 01   .417928E 02   .433051E 02   32.00   .150030E 03   12.50
  .751590E 01   .406752E 02   .451888E 02   33.00   .150042E 03   13.61
  .727016E 01   .398416E 02   .470071E 02   34.00   .150014E 03   14.73
  .703309E 01   .392987E 02   .487612E 02   35.00   .150012E 03   15.85
  .703309E 01   .392987E 02   .487612E 02   36.00   .150012E 03   15.85

 140 EXIT

?OFF
OFF AT 09:21  06/17
COMPUTE SEC. = 310.8
CONNECT MIN. = 46
```

Computer Print-out No. 3

```
 ?BASIC VIC
 RUN
 E    E2    A1    A2    A3    N    I2    P    R    R2
 !28,1.6,.5,.93,.845,3,7.14,190,1.96,.002
        E0              I3              R3              R1              N1
   .390600E 02   .797166E 02   .288404E 01   .123530E 01   .320880E 02
  X      Y      Z      A      B      C
 !3.3,3.7,.1,33,36,1
        I2              I3              E0              N1              P              R0
 N=  3.30
   .754420E 01   .783592E 02   .407801E 02   33.00   .190061E 03   8.75
   .726153E 01   .764653E 02   .427142E 02   34.00   .190055E 03   9.60
   .699391E 01   .751612E 02   .445454E 02   35.00   .190067E 03   10.44
   .673721E 01   .742756E 02   .463018E 02   36.00   .190059E 03   11.28
   .673721E 01   .742756E 02   .463018E 02   37.00   .190059E 03   11.28
 N=  3.40
   .775389E 01   .788103E 02   .407109E 02   33.00   .190069E 03   8.72
   .747234E 01   .766275E 02   .426894E 02   34.00   .190032E 03   9.59
   .720615E 01   .750646E 02   .445601E 02   35.00   .190011E 03   10.45
   .695273E 01   .740184E 02   .463409E 02   36.00   .190044E 03   11.30
   .695273E 01   .740184E 02   .463409E 02   37.00   .190044E 03   11.30
 N=  3.50
   .795544E 01   .794166E 02   .406179E 02   33.00   .190073E 03   8.68
   .767488E 01   .769410E 02   .426415E 02   34.00   .190002E 03   9.57
   .741177E 01   .752010E 02   .445393E 02   35.00   .190016E 03   10.44
   .715977E 01   .739127E 02   .463570E 02   36.00   .190007E 03   11.31
   .715977E 01   .739127E 02   .463570E 02   37.00   .190007E 03   11.31
 N=  3.60
   .814726E 01   .800724E 02   .405173E 02   33.00   .190009E 03   8.64
   .787153E 01   .774909E 02   .425575E 02   34.00   .190048E 03   9.53
   .760946E 01   .754812E 02   .444966E 02   35.00   .190016E 03   10.42
   .736038E 01   .740274E 02   .463395E 02   36.00   .190032E 03   11.30
   .736038E 01   .740274E 02   .463395E 02   37.00   .190032E 03   11.30
 N=  3.70
   .833407E 01   .809747E 02   .403789E 02   33.00   .190032E 03   8.58
   .805895E 01   .780899E 02   .424659E 02   34.00   .190029E 03   9.49
   .779964E 01   .758987E 02   .444330E 02   35.00   .190020E 03   10.39
   .755335E 01   .742788E 02   .463013E 02   36.00   .190055E 03   11.28
   .755335E 01   .742788E 02   .463013E 02   37.00   .190055E 03   11.28

 140 EXIT
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Computer Print-out No. 4

POWER CONDITIONER OPERATING CHARACTERISTICS

Output Voltage – 28 VDC ± 0.06%

Maximum Ripple – 50 MV Peak-to-Peak

Efficiency – 78% at 135 Watt Load (Battery Open Ckt. Voltage = 1.6 V)

Battery Current – 75 Amperes at 135 Watt Load & Open Ckt. Voltage = 1.6 V

Battery Charge Current – 5 Amperes ± 3%

Maximum Output Load for 5 Amp Charge Current – 40 Watts

Overload Current Set – 100 Amperes

Degraded Cell Set – 1.2 VDC

Maximum Charge Voltage Set – 1.995 VDC